Technical Reference Guide

HP Compaq dc7100 and dx6100 Series Business Desktop Computers

Document Part Number: 361834-001

August 2004

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Technical Reference Guide

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First Edition (August 2004)

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Contents

1 Introduction

2 System Overview

3 Processor/Memory Subsystem

4 System Support

5 Input/Output Interfaces

6 Integrated Graphics Subsystem

7 Power and Signal Distribution

8 BIOS ROM

1

Introduction

1.1 About this Guide

This guide provides technical information about HP Compaq dx7100 and dc6100 series personal computers that feature the Intel Pentium 4 processor and the Intel 915G chipset. This document describes in detail the system's design and operation for programmers, engineers, technicians, and system administrators, as well as end-users wanting detailed information.

The chapters of this guide primarily describe the hardware and firmware elements and primarily deal with the system board and the power supply assembly. The appendices contain general data such as error codes and information about standard peripheral devices such as keyboards, graphics cards, and communications adapters.

This guide can be used either as an online document or in hardcopy form.

1.1.1 Online Viewing

Online viewing allows for quick navigating and convenient searching through the document. A color monitor will also allow the user to view the color shading used to highlight differential data. A softcopy of the latest edition of this guide is available for downloading in .pdf file format at the URL listed below:

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Viewing the file requires a copy of Adobe Acrobat Reader available at no charge from Adobe Systems, Inc. at the following URL:

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When viewing with Adobe Acrobat Reader, click on the () icon or “Bookmarks” tab to display the navigation pane for quick access to particular places in the guide.

1.1.2 Hardcopy

A hardcopy of this guide may be obtained by printing from the .pdf file. The document is designed for printing in an 8 ½ x 11-inch format. Note that printing in black and white will lose color shading properties.

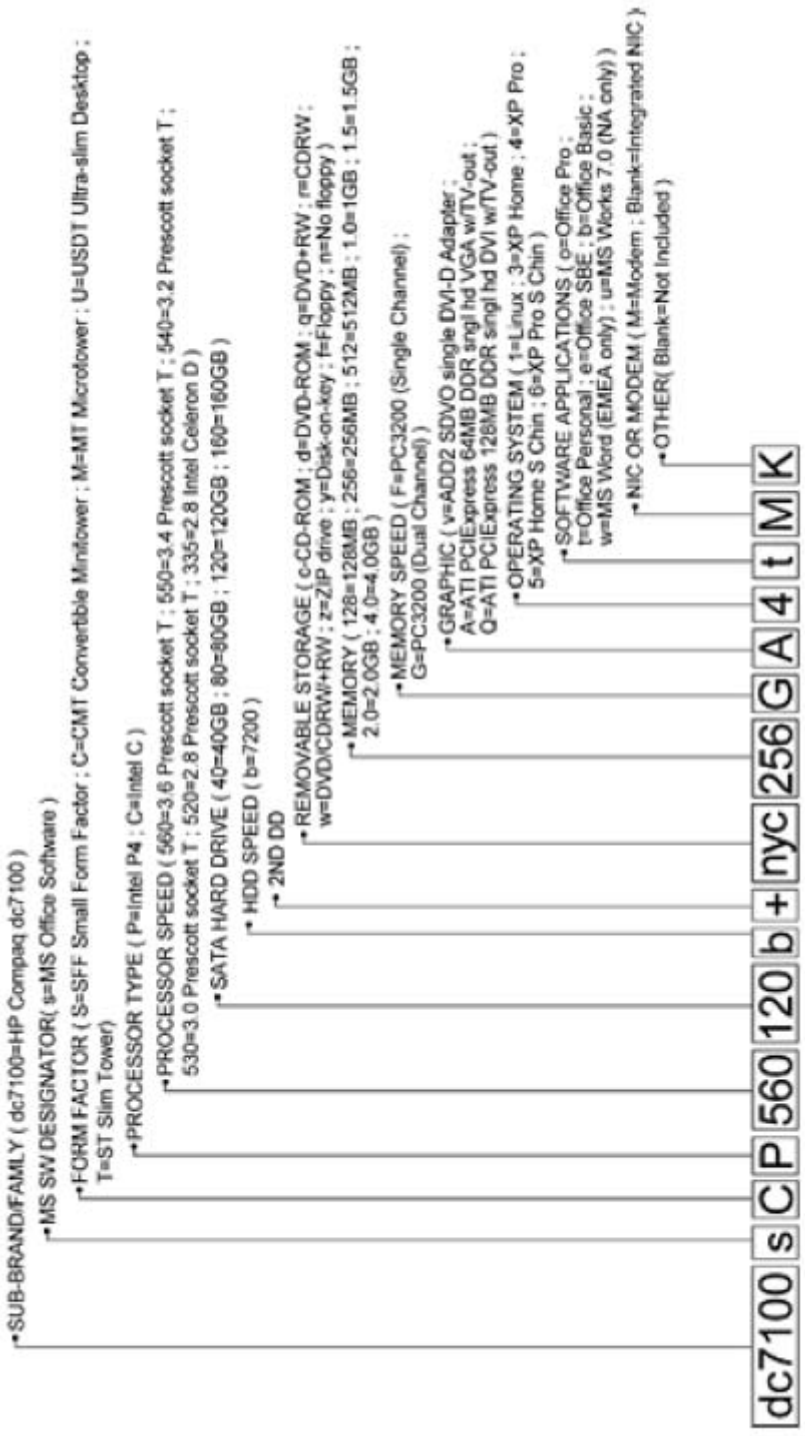
1.2 Additional Information Sources

For more information on components mentioned in this guide refer to the indicated manufacturers' documentation, which may be available at the following online sources:

- HP Corporation: www.hp.com
- Intel Corporation: www.intel.com
- Standard Microsystems Corporation: www.smsc.com
- USB user group: www.usb.org

1.3 Model Numbering Convention

The model numbering convention or HP systems is as follows:



1.4 Serial Number

The unit's serial number is located on a sticker placed on the exterior cabinet. The serial number is also written into firmware and may be read with HP Diagnostics or Insight Manager utilities.

1.5 Notational Conventions

The notational guidelines used in this guide are described in the following subsections.

1.5.1 Values

Hexadecimal values are indicated by a numerical or alpha-numerical value followed by the letter "h." Binary values are indicated by a value of ones and zeros followed by the letter "b." Numerical values that have no succeeding letter can be assumed to be decimal unless otherwise stated.

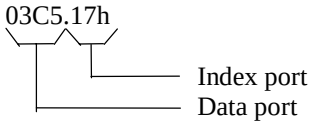
1.5.2 Ranges

Ranges or limits for a parameter are shown using the following methods:

Example A:	Bits <7..4> = bits 7, 6, 5, and 4.
Example B:	IRQ3-7, 9 = IRQ signals 3 through 7, and IRQ signal 9

1.5.3 Register Notation and Usage

This guide uses standard Intel naming conventions in discussing the microprocessor's (CPU) internal registers. Registers that are accessed through programmable I/O using an indexing scheme are indicated using the following format:



In the example above, register 03C5.17h is accessed by writing the index port value 17h to the index address (03C4h), followed by a write to or a read from port 03C5h.

1.5.4 Bit Notation and Byte Values

Bit designations are labeled between brackets (i.e., "bit <0 >"). Binary values are shown with the most significant bit (MSb) on the far left, least significant bit (LSb) at the far right. Byte values in hexadecimal are also shown with the MSB on the left, LSB on the right.

1.6 Common Acronyms and Abbreviations

Table 1-1 lists the acronyms and abbreviations used in this guide.

Table 1-1
Acronyms and Abbreviations

Acronym or Abbreviation	Description
A	ampere
AC	alternating current
ACPI	Advanced Configuration and Power Interface
A/D	analog-to-digital
ADC	Analog-to-digital converter
ADD or ADD2	Advanced digital display (card)
AGP	Accelerated graphics port
API	application programming interface
APIC	Advanced Programmable Interrupt Controller
APM	advanced power management
AOL	Alert-On-LAN™
ASIC	application-specific integrated circuit
ASF	Alert Standard Format
AT	1. attention (modem commands) 2. 286-based PC architecture
ATA	AT attachment (IDE protocol)
ATAPI	ATA w/packet interface extensions
AVI	audio-video interleaved
AVGA	Advanced VGA
AWG	American Wire Gauge (specification)
BAT	Basic assurance test
BCD	binary-coded decimal
BIOS	basic input/output system
bis	second/new revision
BNC	Bayonet Neill-Concelman (connector type)
bps or b/s	bits per second
BSP	Bootstrap processor
BTO	Built to order
CAS	column address strobe
CD	compact disk
CD-ROM	compact disk read-only memory
CDS	compact disk system
CGA	color graphics adapter

Table 1-1
Acronyms and Abbreviations

Acronym or Abbreviation	Description
Ch	Channel, chapter
cm	centimeter
CMC	cache/memory controller
CMOS	complimentary metal-oxide semiconductor (configuration memory)
Cntlr	controller
Cntrl	control
codec	1. coder/decoder 2. compressor/decompressor
CPQ	Compaq
CPU	central processing unit
CRIMM	Continuity (blank) RIMM
CRT	cathode ray tube
CSM	1. Compaq system management 2. Compaq server management
DAC	digital-to-analog converter
DC	direct current
DCH	DOS compatibility hole
DDC	Display Data Channel
DDR	Double data rate (memory)
DIMM	dual inline memory module
DIN	Deutche IndustriNorm (connector type)
DIP	dual inline package
DMA	direct memory access
DMI	Desktop management interface
dpi	dots per inch
DRAM	dynamic random access memory
DRQ	data request
DVI	Digital video interface
dword	Double word (32 bits)
EDID	extended display identification data
EDO	extended data out (RAM type)
EEPROM	electrically eraseable PROM
EGA	enhanced graphics adapter
EIA	Electronic Industry Association
EISA	extended ISA
EPP	enhanced parallel port
EIDE	enhanced IDE

Table 1-1
Acronyms and Abbreviations

Acronym or Abbreviation	Description
ESCD	Extended System Configuration Data (format)
EV	Environmental Variable (data)
ExCA	Exchangeable Card Architecture
FIFO	first in/first out
FL	flag (register)
FM	frequency modulation
FPM	fast page mode (RAM type)
FPU	Floating point unit (numeric or math coprocessor)
FPS	Frames per second
ft	Foot/feet
GB	gigabyte
GMCH	Graphics/memory controller hub
GND	ground
GPIO	general purpose I/O
GPOC	general purpose open-collector
GART	Graphics address re-mapping table
GUI	graphic user interface
h	hexadecimal
HW	hardware
hex	hexadecimal
Hz	Hertz (cycles-per-second)
ICH	I/O controller hub
IDE	integrated drive element
IEEE	Institute of Electrical and Electronic Engineers
IF	interrupt flag
I/F	interface
IGC	integrated graphics controller
in	inch
INT	interrupt
I/O	input/output
IPL	initial program loader
IrDA	Infrared Data Association
IRQ	interrupt request
ISA	industry standard architecture

Table 1-1
Acronyms and Abbreviations

Acronym or Abbreviation	Description
Kb/KB	kilobits/kilobytes (x 1024 bits/x 1024 bytes)
Kb/s	kilobits per second
kg	kilogram
KHz	kilohertz
kV	kilovolt
lb	pound
LAN	local area network
LCD	liquid crystal display
LED	light-emitting diode
LPC	Low pin count
LSI	large scale integration
LSb/LSB	least significant bit/least significant byte
LUN	logical unit (SCSI)
m	Meter
MCH	Memory controller hub
MMX	multimedia extensions
MPEG	Motion Picture Experts Group
ms	millisecond
MSb/MSB	most significant bit/most significant byte
mux	multiplex
MVA	motion video acceleration
MVW	motion video window
n	variable parameter/value
NIC	network interface card/controller
NiMH	nickel-metal hydride
NMI	non-maskable interrupt
NRZI	Non-return-to-zero inverted
ns	nanosecond
NT	nested task flag
NTSC	National Television Standards Committee
NVRAM	non-volatile random access memory
OS	operating system
PAL	1. programmable array logic 2. phase alternating line
PATA	Parallel ATA

Table 1-1
Acronyms and Abbreviations

Acronym or Abbreviation	Description
PC	Personal computer
PCA	Printed circuit assembly
PCI	peripheral component interconnect
PCI-E	PCI Express
PCM	pulse code modulation
PCMCIA	Personal Computer Memory Card International Association
PEG	PCI express graphics
PFC	Power factor correction
PIN	personal identification number
PIO	Programmed I/O
PN	Part number
POST	power-on self test
PROM	programmable read-only memory
PTR	pointer
RAM	random access memory
RAS	row address strobe
rcvr	receiver
RDRAM	(Direct) Rambus DRAM
RGB	red/green/blue (monitor input)
RH	Relative humidity
RMS	root mean square
ROM	read-only memory
RPM	revolutions per minute
RTC	real time clock
R/W	Read/Write
SATA	Serial ATA
SCSI	small computer system interface
SDR	Singles data rate (memory)
SDRAM	Synchronous Dynamic RAM
SDVO	Serial digital video out
SEC	Single Edge-Connector
SECAM	sequential colour avec memoire (sequential color with memory)
SF	sign flag
SGRAM	Synchronous Graphics RAM

Table 1-1
Acronyms and Abbreviations

Acronym or Abbreviation	Description
SIMD	Single instruction multiple data
SIMM	single in-line memory module
SMART	Self Monitor Analysis Report Technology
SMI	system management interrupt
SMM	system management mode
SMRAM	system management RAM
SPD	serial presence detect
SPDIF	Sony/Philips Digital Interface (IEC-958 specification)
SPN	Spare part number
SPP	standard parallel port
SRAM	static RAM
SSE	Streaming SIMD extensions
STN	super twist pneumatic
SVGA	super VGA
SW	software
TAD	telephone answering device
TAFI	Temperature-sensing And Fan control Integrated circuit
TCP	tape carrier package
TF	trap flag
TFT	thin-film transistor
TIA	Telecommunications Information Administration
TPE	twisted pair ethernet
TPI	track per inch
TTL	transistor-transistor logic
TV	television
TX	transmit
UART	universal asynchronous receiver/transmitter
UDMA	Ultra DMA
URL	Uniform resource locator
us/µs	microsecond
USB	Universal Serial Bus
UTP	unshielded twisted pair
V	volt
VAC	Volts alternating current

Table 1-1
Acronyms and Abbreviations

Acronym or Abbreviation	Description
VDC	Volts direct current
VESA	Video Electronic Standards Association
VGA	video graphics adapter
VLSI	very large scale integration
VRAM	Video RAM
W	watt
WOL	Wake-On-LAN
WRAM	Windows RAM
ZF	zero flag
ZIF	zero insertion force (socket)

2

System Overview

2.1 Introduction

The HP Compaq dc7100 and dx6100 Series Business Desktop Computers (Figure 2-1) deliver an outstanding combination of manageability, serviceability, and compatibility for enterprise environments. Based on the Intel Pentium 4 processor with the Intel 915G Chipset, these systems emphasize performance along with industry compatibility. These models feature architectures incorporating the PCI bus. All models are easily upgradeable and expandable to keep pace with the needs of the office enterprise.

Model release dates may vary be region and/or geographical area.

HP Compaq dc7100 USDT

HP Compaq dc7100 SFF

HP Compaq dx6100 ST

HP Compaq dx6100 MT

HP Compaq dc7100 CMT

Figure 2-1. HP Compaq dx6100 and dc7100 Series Business Desktop Computers

This chapter includes the following topics:

Features And Options

This section describes the standard features.

2.2.1 Standard Features

The following standard features are included on all series:

- Intel Pentium 4 processor in LGA775 (Socket T) package
- Integrated graphics controller
- PC2700 and PC3200 support, with PC3200 DIMMs supplied,
- IDE controller providing serial and parallel ATA support
- Hard drive fault prediction
- Eight USB 2.0 ports
- Audio processor with one headphone output, one microphone input, and one line input
- Network interface controller providing 10/100/1000Base T support
- Plug 'n Play compatible (with ESCD support)
- Intelligent Manageability support
- Energy Star compliant
- Security features including:
  - Flash ROM Boot Block
  - Diskette drive disable, boot disable, write protect
  - Power-on password
  - Administrator password
  - Serial/parallel port disable
- PS/2 enhanced keyboard
- PS/2 scroll mouse

Table 2-1 shows the differences in features between the different PC series based on form factor:

Table 2-1
Difference Matrix by Form Factor

	USDT	SFF	ST	MT	CMT
Series	dc7100	dc7100	dx6100	dx6100	dc7100
System Board Type	custom	custom	custom	μATX	μATX
Serial and parallel ports	Optional [1]	Standard	Standard	Standard	Standard
Memory:					
# of sockets	3	4	4	4	4
Maximum memory	3 GB	4 GB	4 GB	4 GB	4 GB
Drive bays:					
Externally accessible	1	2	2	3	4
Internal	1	1	1	2	2
PCI Express slots:					
x16 graphics	0	1 [2] [3]	1 [2] [3]	1 [4]	1 [4]
x1	0	1 [3]	1 [3]	1	1
PCI 2.3 slots	1full-height	2 half-height or 2 full-height [5]	2 half-height or 2 full-height [5]	2 full-height	2 full-height or 4 full-height [6]
MultiBay	Standard	Optional [7]	Optional [7]	not supported	Optional [7]
Smart Cover Sensor / Lock	Sensor only	Both	No	No	Both
Power Supply:					
Power rating	200-watt	240-watt	240-watt	300-watt [8]	340-watt
PFC	Active PFC	Active PFC	Active PFC	Passive PFC	Active PFC
Auto-ranging	Yes	Yes	Yes	No	Yes

NOTE:

[1] Supported on system board. Requires optional cable/bracket assembly.

[2] Accepts low-profile, reversed-layout ADD2/SDVO card: height = 2.5 in., length = 6.6 in.

[3] Slot not accessible in configuration using PCI riser card.

[4] Accepts standard height, normal (non-reversed) layout ADD2/SDVO card: height = 4.2 in., length = 10.5 in.

[5] Riser card configuration is a field option. Full-height PCI slots provided with configuration using PCI riser card.
Half-height dimensions: height = 2.5 in., length = 6.6 in.
Full-hieght dimensions: height = 4.2 in., length = 6.875 in

[6] PCI expansion board required for 4-slot support.
Full-height dimensions:

[7] Requires adapter.

[8] Some MT SKUs shipped with 340-watt power supplies.

2.3 Mechanical Design

This guide covers six form factors:

- Ultra Slim Desktop (USDT)—Very slim design that can be used in a tradition desktop (horizontal) orientation or as a small tower mounted in the supplied tower stand.
- Small Form Factor (SFF)—A small-footprint desktop requiring minimal desk space.
- Slim Tower (ST)—Slim design that can be used in a tradition desktop (horizontal) orientation or as a small tower mounted in the supplied tower stand.
- Microtower (MT)- A low-height tower that requires less vertical space than a minitower.
- Convertible Minitower (CMT) —an ATX-type unit providing the most expandability and being adaptable to desktop (horizontal) or floor-standing (vertical) placement.

The following subsections describe the mechanical (physical) aspects of models.

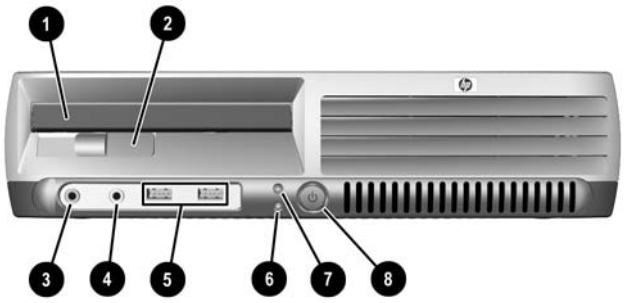
CAUTION: Voltages are present within the system unit whenever the unit is plugged into a live AC outlet, regardless of the system's "Power On" condition. Always disconnect the power cable from the power outlet and/or from the system unit before handling the system unit in any way.

The following information is intended primarily for identification purposes only. Before servicing these systems, refer to the applicable Service Reference Guide. Service personnel should review training materials also available on these products.

2.3.1 Cabinet Layouts

Front Views

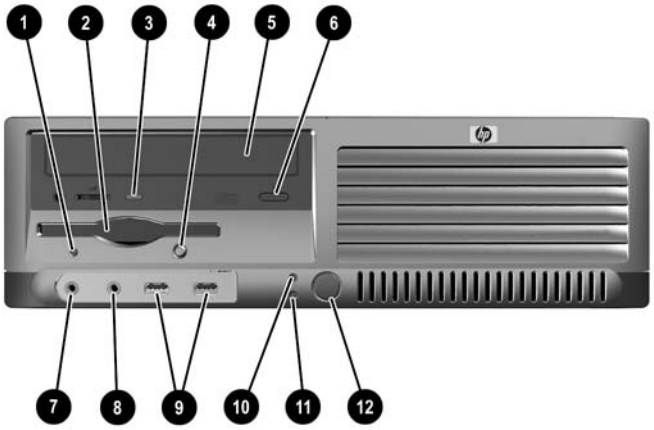
Figure 2-2 shows the front panel components of the Ultra Slim Desktop (USDT) format factor.



Item	Description	Item	Decription
1	MultiBay device bay	5	USB ports 7, 8
2	MultiBay device eject lever	6	Power LED
3	Microphone audio In jack	7	MultiBay device / HD activity LED
4	Headphone audio Out jack	8	Power button

Figure 2-2. HP Compaq dc7100 USDT Front View

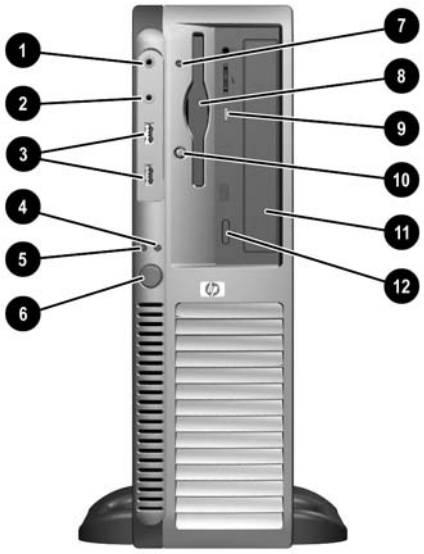
Figure 2-3 shows the front panel components of the Small Form Factor (SFF).



Item	Description	Item	Decription
1	Diskette drive activity LED	7	Microphone audio In jack
2	Diskette drive media door	8	Headphone audio Out jack
3	CD-ROM drive acitvity LED	9	USB ports 7, 8
4	Diskette drive eject button	10	Hard drive activity LED
5	CD-ROM media tray	11	Power LED
6	CD-ROM drive open/close button	12	Power button

Figure 2-3. HP Compaq dc7100 SFF Front View

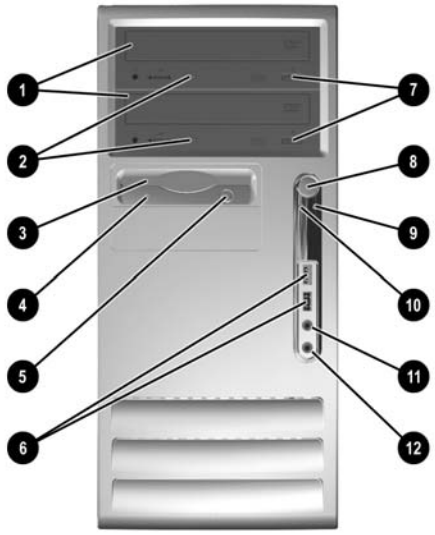
Figure 2-4 shows the front panel components of the Slim Tower (ST) form factor.



Item	Description	Item	Decription
1	Micorphone audio In jack	7	Diskette drive activity LED
2	Headphone audio Out jack	8	Diskette media door
3	USB ports 7, 8	9	CD-ROM drive acitvity LED
4	hard drive activity LED	10	Diskette drive eject button
5	Power LED	11	CD-ROM media tray
6	Power button	12	CD-ROM drive open/close button

Figure 2-4. HP Compaq dx6100 ST Front View

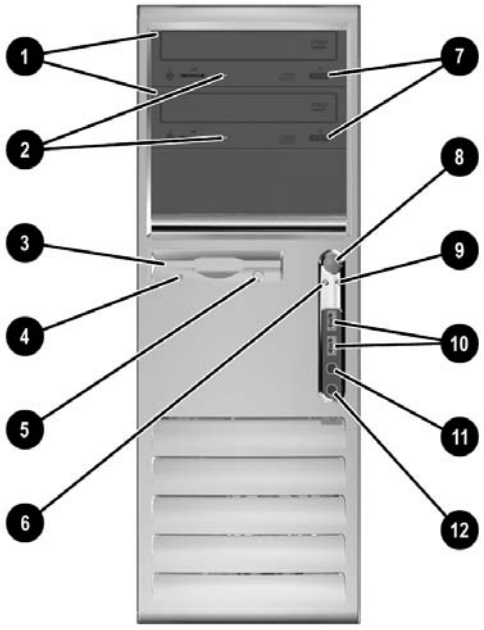
Figure 2-5 shows the front panel components of the microtower (uT) form factor.



Item	Description	Item	Decription
1	CD-ROM drive	7	CD-ROM drive open/close button
2	CD-ROM drive activity LED	8	Power button
3	Diskette drive media door	9	Power LED
4	Diskette drive activity LED	10	Hard drive activity LED
5	Diskette drive eject button	11	Headphone audio Out jack
6	USB ports 7, 8	12	Microphone audio In jack

Figure 2-5. HP Compaq dx6100 MT Front View

Figure 2-6 shows the front panel components of the Convertable Minitower (CMT) form factor.

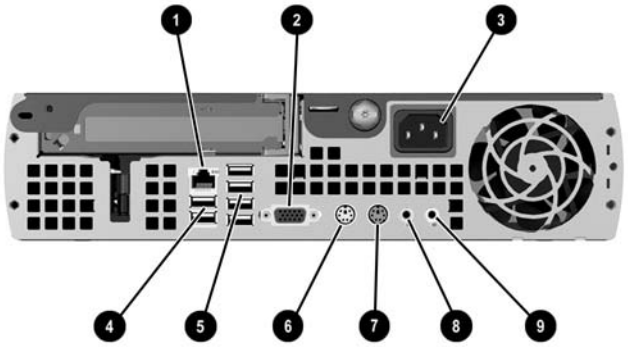


Item	Description	Item	Decription
1	CD-ROM drive	7	CD-ROM drive open/close button
2	CD-ROM drive activity LED	8	Power button
3	Diskette drive media door	9	Power LED
4	Diskette drive activity LED	10	USB ports 7, 8
5	Diskette drive eject button	11	Headphone audio Out jack
6	Hard drive activity LED	12	Microphone audio In jack

Figure 2-6. HP Compaq dc7100 CMT Front View

Rear Views

Figure 2-7 shows the rear view of the USDT form factor.

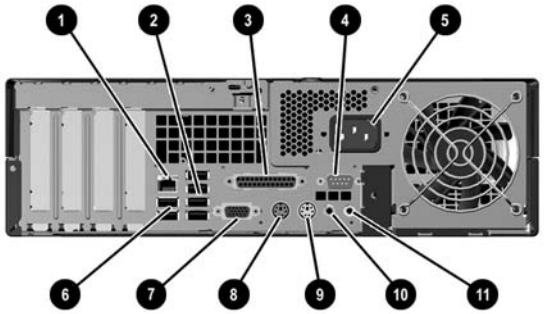


Item	Description	Item	Description
1	NIC (LAN) connector (RJ-45)	6	Mouse connector (PS/2)
2	VGA monitor connector (DB-15)	7	Keyboard connector (PS/2)
3	AC input connector	8	Line audio In
4	USB ports 1, 2	9	Headphone / Speaker audio Out
5	USB ports 3 - 6	--	--

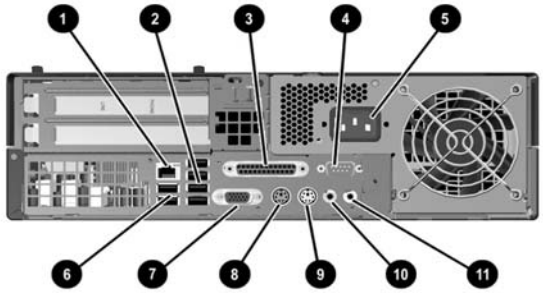
Figure 2-7. HP Compaq dc7100 USDT, Rear View

Figure 2-8 shows the rear views of the SFF form factor. Two configurations are available:

- Without cardcage - Accepts two half-height PCI 2.3 cards, two half-height PCI Express cards
- With card cage - Accepts two full-height PCI 2.3 cards only



SFF chassis without card cage



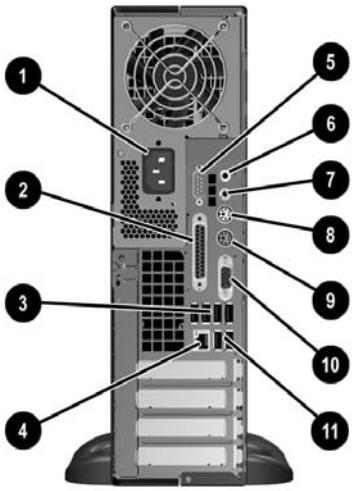
SFF Chassis with card cage

Item	Description	Item	Description
1	NIC (LAN) connector (RJ-45)	7	VGA monitor connector (DB-15)
2	USB ports 3 - 6	8	Mouse connector (PS/2)
3	Parallel port (DB-25)	9	Keyboard connector (PS/2)
4	Serial port (DB-9)	10	Line audio In
5	AC input connector	11	Headphone / Speaker audio Out
6	USB ports 1, 2	–	–

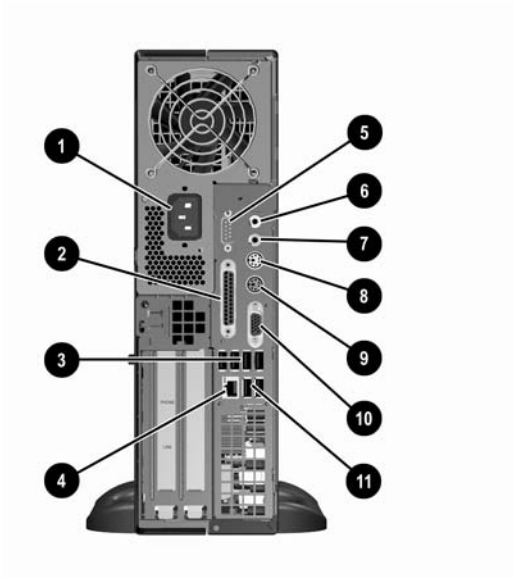
Figure 2-8. HP Compaq dc7100 SFF, Rear Views

Figure 2-9 shows the rear views of the ST form factor. Two configurations are available:

- Without cardcage - Accepts two half-height PCI 2.3 cards, two half-height PCI Express cards
- With card cage - Accepts two full-height PCI 2.3 cards only



ST chassis without card cage

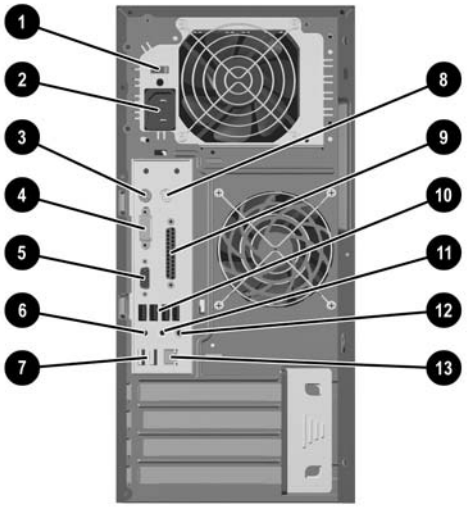


ST chassis with card cage

Item	Description	Item	Description
1	AC input connector	7	Line audio In
2	Parallel port (DB-25)	8	Keyboard connector (PS/2)
3	USB ports 3 - 6	9	Mouse connector (PS/2)
4	NIC (LAN) connector (RJ-45)	10	VGA monitor connector (DB-15)
5	Serial port (DB-9)	11	USB ports 1, 2
6	Headphone / Speaker audio Out	–	–

Figure 2-9. HP Compaq dc7100 ST, Rear Views

Figure 2-10 shows the rear view of the MT form factor.



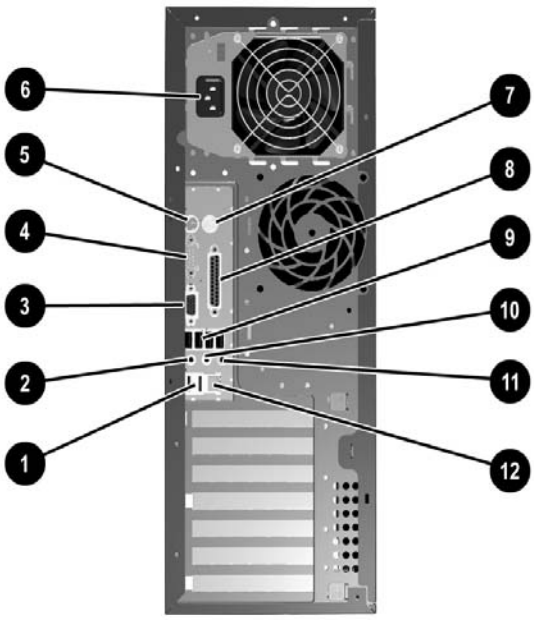
Item	Description	Item	Description
1	AC voltage select switch	8	Mouse connector (PS/2)
2	AC line connector Microphone In jack	9	Parallel port connctor (DB-25)
3	Keyboard connector (PS/2)	10	USB ports 1 - 4
4	Serial port connector (DB-9)	11	Line audio Out jack
5	VGA monitor connector (B-15)	12	Line audio In jack
6	Microphone In jack	13	NIC (LAN) connector (RJ-45)
7	USB ports 5, 6	--	--

NOTE:

[1] Switch not present on SKUs that feature auto-ranging power supply.

Figure 2-10. HP Compaq dx6100 MT, Rear View

Figure 2-11 shows the rear view of the CMT form factor.



Item	Description	Item	Description
1	USB ports 5, 6	7	Mouse connector (PS/2)
2	Microphone audio In	8	Parallel port connector (DB-25)
3	VGA monitor connector (DB-15)	9	USB ports 1-4
4	Serial port connector (DB-9)	10	Line audio Out jack
5	Keyboard connector (PS/2))	11	Line audio In jack
6	AC line connector	12	NIC (LAN) connector (RJ-45)

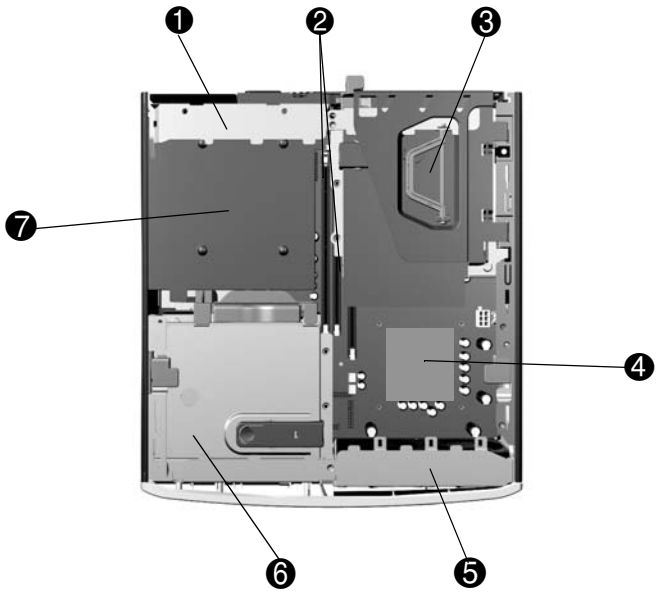
Figure 2-11. HP Compaq dc7100 CMT, Rear View

2.3.2 Chassis Layouts

This section describes the internal layouts of the chassis. For detailed information on servicing the chassis refer to the multimedia training and/or the maintenance and service guide for these systems.

Ulltra Slim Desktop Chassis

The Ultra Slim Desktop (USDT) chassis used for the HP Compaq dc7100 models uses a compact, space-saving form factor.



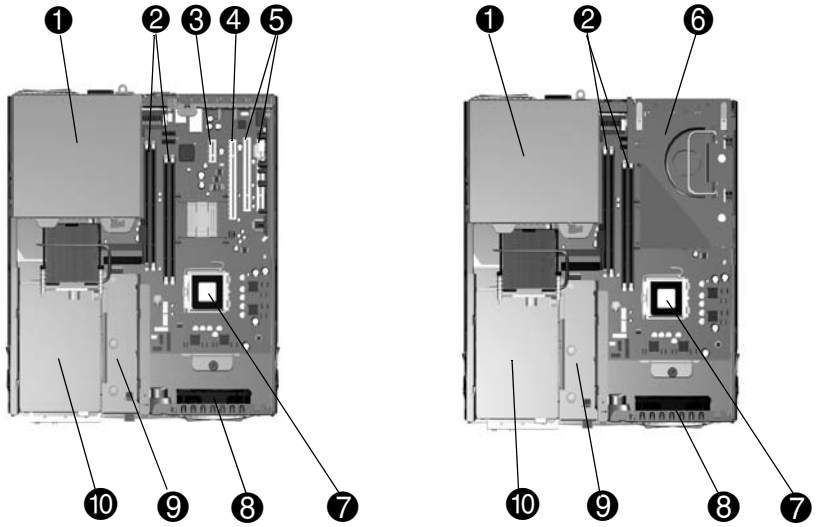
Item	Description	Item	Description
1	Power supply assembly	5	Chassis fan
2	DIMM sockets (3)	6	MultiBay device
3	PCI card cage	7	Hard drive
4	Processor socket	--	--

Figure 2-12. USDT Chassis Layout, TopView

Small Form Factor / Slim Tower Chassis

The chassis layouts for the Small Form Factor (SFF) used for the HP Compaq dc7100 models and the Slim Tower (ST) used for the HP Comapq dx6100 models are shown in Figure 2-13. Features include:

- Tilting drive cage assembly for easy access to processor and memory sockets
- Two configurations:
  - Without card cage:
    - Two half-height, full length PCI 2.3 slots
    - One PCI Express x16 graphics/SDVO slot
    - One PCI Express x1 slot
  - With card cage:
    - Two full-height, full-length PCI 2.3 slots



Chassis without card cage

Chassis with card cage

Item	Description	Item	Description
1	Power supply assembly	6	Card cage
2	DIMM sockets (4)	7	Processor socket
3	PCI Express x1 slot	8	Chassis fan
4	PCI Express x16 graphics/reversed-layout SDVO slot [1]	9	Diskette drive bay
5	PCI 2.3 slots (2)	10	CD-ROM drive bay

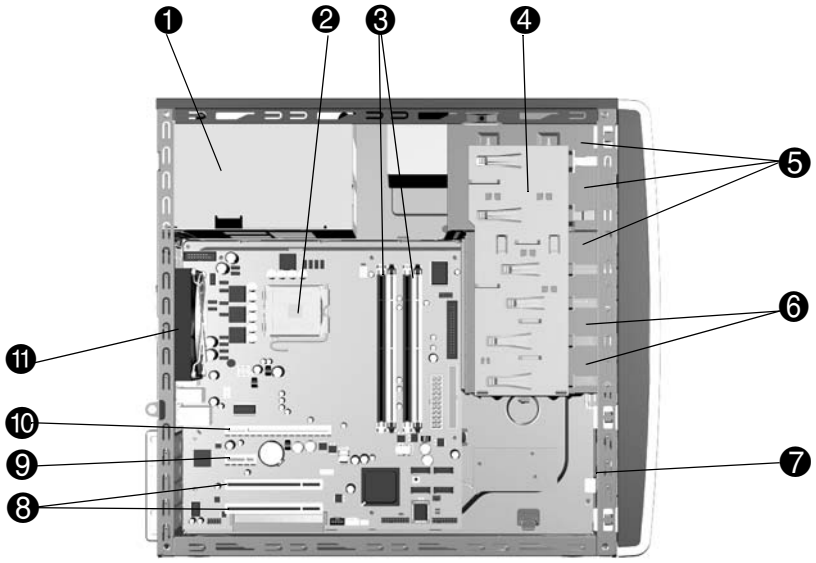
NOTE:
[1] Accepts PCI-E graphics or reversed-layout ADD2 card.

Figure 2-13. SFF / ST Chassis Layout, Top / Right Side Views

Microtower Chassis

Figure 2-14 shows the layout for the Microtower (MT) chassis used for the HP Compaq dx6100 models. Features include:

- Externally accessible drive bay assembly.
- Easy access to expansion slots and all socketed system board components.



Item	Description	Item	Description
1	Power supply assembly	7	Speaker
2	Processor socket	8	PCI 2.3 slots
3	DIMM sockets (4)	9	PCI Express x1 slot
4	DriveLock	10	PCI Express x16 graphics/normal layout SDVO slot [1]
5	Externally accessible drive bays	11	Chassis fan
6	Internally accessible drive bays	–	–

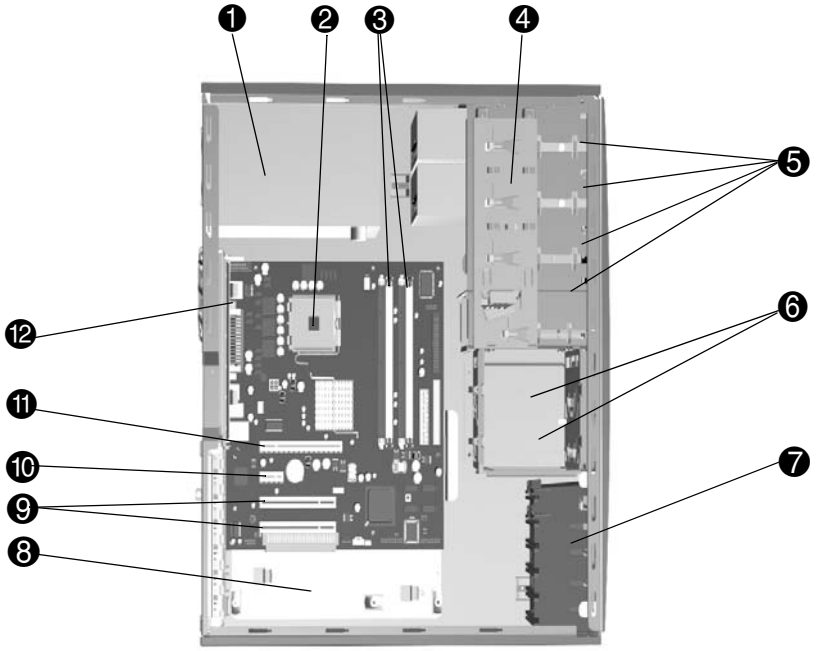
NOTE:
[1] Accepts PCI-E graphics or normal layout ADD2 card.

Figure 2-14. MT Chassis Layout, Left Side View

Convertible Minitower

Figure 2-15 shows the layout for the Convertible Minitower (CMT) chassis in the minitower configuration used for HP Compaq dc7100 models. Features include:

- Externally accessible drive bay assembly may be configured for minitower (vertical) or desktop (horizontal) position.
- Easy access to expansion slots and all socketed system board components.



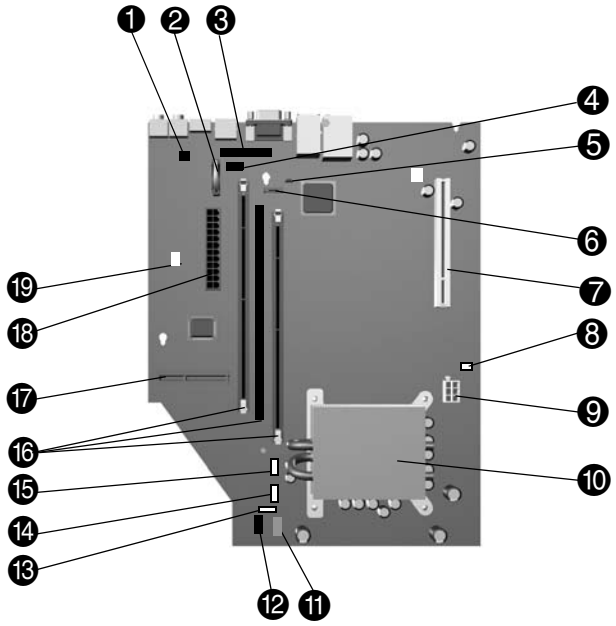
Item	Description	Item	Description
1	Power supply assembly	7	Speaker (inside card guide assembly)
2	Processor socket	8	Expansion board area
3	DIMM sockets (4)	9	PCI 2.3 slots
4	DriveLock	10	PCI Express x1 slot
5	Externally accessible drive bays	11	PCI Express x16 graphics/normal layout SDVO slot [1]
6	Internally accessible drive bays	12	Chassis fan

NOTE:
[1] Accepts PCI-E graphics or normal layout ADD2 card.

Figure 2-15. CMT Chassis Layout, Left Side View (Minitower configuration)

2.3.3 Board Layouts

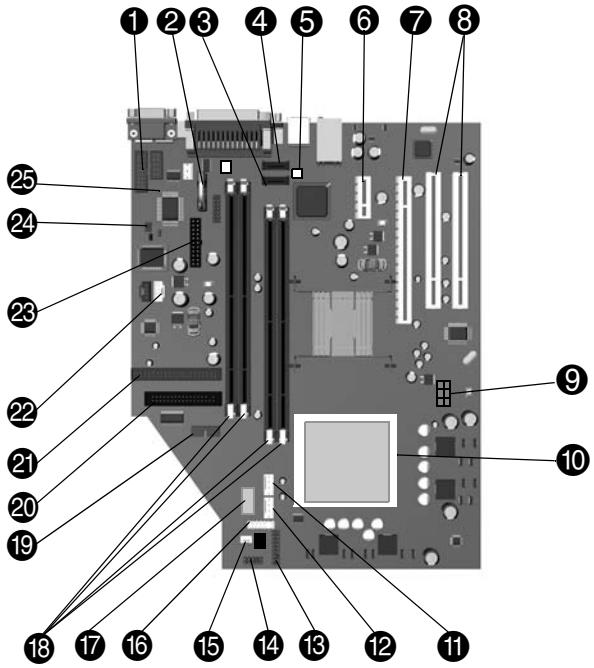
Figures 2-16 through 2-18 show the system and expansion boards for these systems.



Note: See USDT rear chassis illustrations for externally accessible I/O connectors.

Item	Description	Item	Description
1	Hood sense header	11	Power button, power LED, HD LED header
2	Battery	12	Front panel audio connector
3	Parallel port option header	13	Front panel USB port connector
4	Serial port A header	14	Chassis fan, secondary connector
5	Password clear jumper header	15	Chassis fan, primary connector
6	SATA #0 header	16	DIMM sockets (3)
7	PCI 2.3 slot	17	MultiBay riser connector
8	Intenal speaker header	18	Power supply connector
9	Power supply (VccP) connector	19	Auxiliary audio input connector
10	Processor socket	–	–

Figure 2-16. USDT System Board

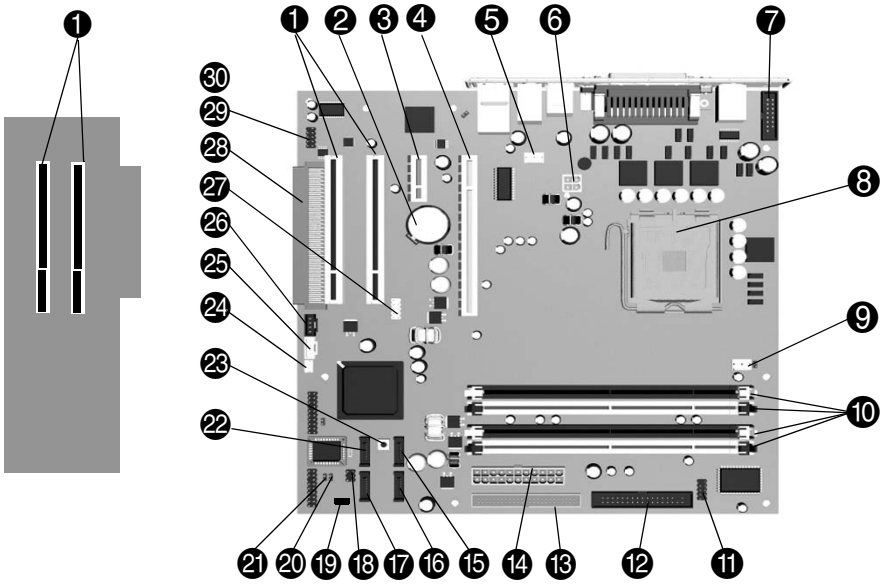


Note: See SFF and ST rear chassis illustrations for externally accessible I/O connectors.

Item	Description	Item	Description
1	Serial port B header	14	Front panel audio header
2	Battery	15	Chassis speaker connector
3	SATA #1 header	16	Front panel USB port connector
4	SATA #0 header	17	MultiBay connector
5	Password jumper	18	DIMM sockets (4)
6	PCI Express x1 slot	19	CD-Audio input connector
7	PCI Express x16 graphics/reversed layout SDVO slot [1]	20	Diskette drive connector
8	PCI 2.3 slots	21	PATA (primary IDE) connector
9	Power supply (VccP) connector	22	Auxiliary audio input connector
10	Processor socket	23	Power supply connector
11	Chassis fan, primary connector	24	Cover lock (solenoid) connector
12	Chassis fan, secondary conenctor	25	Cover sensor connector
13	Power button, power LED, HD LED header	--	--

NOTES:
See SFF and ST rear chassis illustrations for externally accessible I/O connectors
[1] Accepts PCI-E graphics or reversed-layout ADD2 card.

Figure 2-17. SFF / ST System Board



PCI Expansion Board [1] System Board

Item	Description	Item	Description
1	PCI 2.3 slots	16	Serial ATA #2 connector [3]
2	Battery	17	Serial ATA #0 connector
3	PCI Express x1 slot	18	Hood lock header [3]
4	PCI Express x16 graphics slot / normal layout SDVO slot [2]	19	Hood sense header [3]
5	Chassis fan header	20	Password clear jumper header
6	Power supply (VccP) connector	21	Power LED/button, HD LED header
7	Serial port B header [3]	22	Serial ATA #1 connector
8	Processor socket	23	CMOS clear switch
9	Processor fan connector	24	Internal speaker connector
10	DIMM sockets (4)	25	Auxiliary audio inpout connector
11	MultiBay conector [3]	26	CD audio input connector
12	Diskette drive connector	27	Front panel USB port connector
13	Parallel ATA connector	28	PCI expansion board connector [3]
14	Power supply connector	29	Front panel audio connector
15	Serial ATA #3 connector [3]	--	--

NOTES:
See MT and CMT rear chassis illustrations for externally accessible I/O connectors
[1] Applicable to CMT chassis only.
[2] Acepts PCI-E graphics or normal layout ADD2 card.
[3] CMT system boards only.

Figure 2-18. MT / CMT System Board and CMT PCI Expansion Board

2.4 System Architecture

The systems covered in this guide feature an architecture based on the Intel Pentium 4 processor and the Intel 915G chipset (Figure 2-11). These systems allow processor upgrading with the Intel Pentium 4 family and offer flexibility in expansion capabilities.

All systems covered in this guide include the following key components:

- Intel Pentium 4 with Hyper-Threading technology, 32-KB L1 cache and 1-MB L2 cache.
- Intel 915G/GV chipset - Includes 82915G or 82915GV GMCH north bridge and 82801 ICH6 south bridge including an integrated graphics controller, dual-channel DDR SDRAM controller, serial and parallel ATA controllers, USB 2.0 controller, and PCI controller supporting PCI 2.3 devices.
- SMC 47B397 super I/O controller supporting PS/2 keyboard and mouse peripherals
- AD1981B audio controller supporting line in, speaker out, and headphone out
- Broadcom BCM5751 10/100/1000 network interface controller

The 915G/GV chipset provides a major portion of system functionality. Designed to compliment the latest Intel Pentium 4 processors, the chipset serves the processor through a 800-MB Front-Side Bus (FSB). Communication between the GMCH and ICH6 components occurs through the Direct Media Interface (DMI). The SFF, ST, MT, and CMT form factors use the integrated graphics controller of the 82915G that may be upgraded through a PCI Express x16 graphics slot. All systems include a PCI 2.3 slot, and feature as standard a serial ATA (SATA) hard drive with support for legacy parallel ATA 100 devices including a MultiBay device.

Table 2-2 lists the differences between models.

Table 2-2.
Architectural Differences By Form Factor

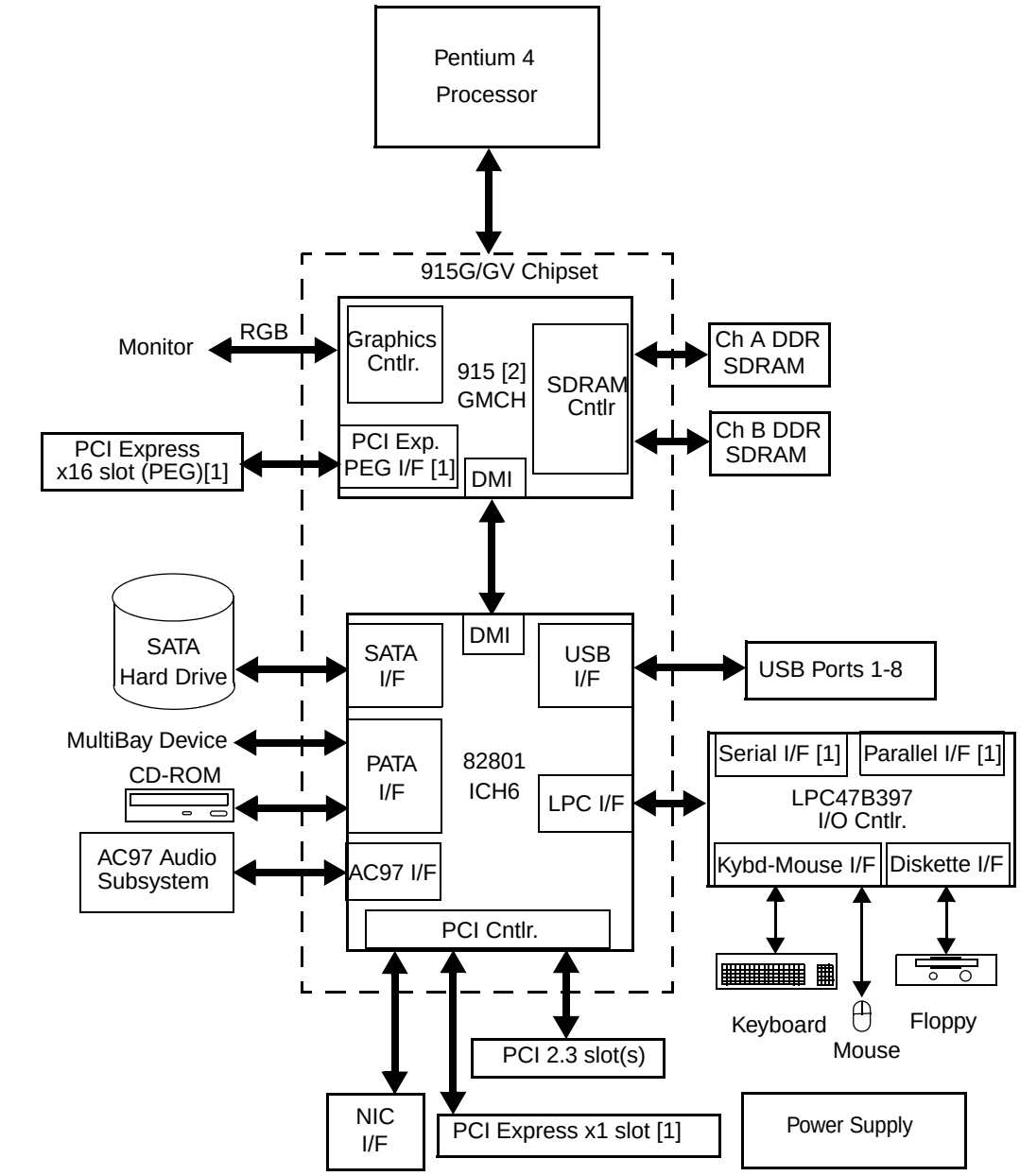
Model	USDT	SFF	ST	MT	CMT
Chipset	915GV	915G	915G	915G	915G
Memory sockets	3	4	4	4	4
Graphics upgrade	PCI 2.3 card only	PCI-E or PCI 2.3 card	PCI-E or PCI 2.3 card	PCI-E or PCI 2.3 card	PCI-E or PCI 2.3 card
PCI Express x16 graphics slot?	No	Yes [1]	Yes [1]	Yes	Yes
PCI Express x1 slot?	No	Yes [1]	Yes [1]	Yes	Yes
Serial / parallel ports	Optional [2]	Standard [3]	Standard [3]	Standard [3]	Standard [3]
SATA interfaces	1	2	2	4	4

Notes:

[1] Slot not accessible if PCI 2.3 full-height riser is installed.

[2] Requires adapter.

[3] 2nd serial port requires adapter.



Note:

[1] SFF, ST, MT, and CMT form factors only.
[2] 82915GV for USDT form factor
82915G for SFF. ST. MT, and CMT form factors

Figure 2-19 System Architecture, Block diagram

2.4.1 Intel Pentium 4 Processor

The models covered in this guide feature the Intel Pentium 4 processor with Hyper-Threading technology. This processor is backward-compatible with software written for the Pentium III, Pentium II, Pentium MMX, Pentium Pro, Pentium, and x86 microprocessors. The processor architecture includes a floating-point unit, 32-KB first and 1-MB secondary caches, and enhanced performance for multimedia applications through the use of multimedia extension (MMX) instructions. Also included are streaming SIMD extensions (SSE and SSE2) for enhancing 3D graphics and speech processing performance. The Pentium 4 processor features Net-Burst Architecture that uses hyper-pipelined technology and a rapid-execution engine that runs at twice the processor's core speed.

These systems employ a zero-insertion-force (ZIF) Socket-T designed for mounting an LGA775 processor package (Figure 2-20).

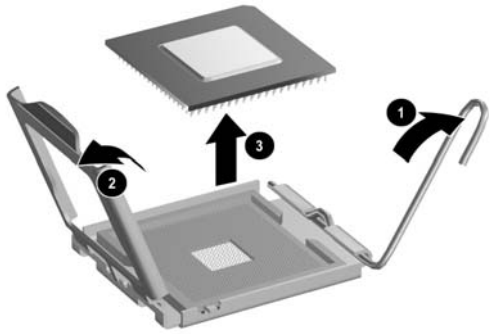


Figure 2-20. Processor Socket and Processor Package

To remove the processor:

1. Remove the processore heat sink/fan assembly (not shown).
2. Release the locking lever (❶) by first pushing down, then out and up.
3. Pull up the securing frame (❷).
4. Grasp the processor (❸) by the edges and lift straight up from the socket.

The processor heatsink/fan assembly mounting differs between form factors. Always use the same assembly or one of the same type when replacing the processor. Refer to the applicable Service Reference Guide for detailed removal and replacement procedures of the heatsink/fan assembly and the processor.

2.4.2 Chipset

The chipset consists of a Graphics Memory Controller Hub (GMCH), an enhanced I/O controller hub (ICH), and a firmware hub (FWH). Table 2-3 compares the functions provided by the chipsets.

Table 2-3
Chipset Components

Components	Function
82915G/GV GMCH	Intel Graphics Media Accelerator 900 (integrated graphics controller) PCI Express x16 graphics interface (915G only) SDRAM controller supporting unbuffered, non-ECC PC2700/PC3200 DDR 533-, or 800-MHz FSB
82801EB ICH6	PCI 2.3 bus I/F PCI Express x1 LPC bus I/F SMBus I/F IDE I/F with SATA and PATA support AC '97 controller RTC/CMOS IRQ controller Power management logic USB 1.1/2.0 controllers supporting eight (8) ports
82802 FWH [1]	Loaded with HP/Compaq BIOS

NOTE:

[1] Or equivalent component.

2.4.3 Support Components

Input/output functions not provided by the chipset are handled by other support components. Some of these components also provide “housekeeping” and various other functions as well. Table 2-4 shows the functions provided by the support components.

Table 2-4
Support Component Functions

Component Name	Function
LPC47B397 I/O Controller	Keyboard and pointing device I/F Diskette I/F Serial I/F (COM1and COM2) Parallel I/F (LPT1, LPT2, or LPT3) PCI reset generation Interrupt (IRQ) serializer Power button and front panel LED logic GPIO ports Processor over tempurature monitoring Fan control and monitoring Power supply voltage monitoring SMBus and Low Pin Count (LPC) bus I/F
BCM5751 Ethernet Controller	10/100/1000 Fast Ethernet network interface controller.
AD1981B Audio Codec	Audio mixer Digital-to-analog converter Analog-to-digital converter Analog I/O 6-channel audio support

2.4.4 System Memory

These systems implement a dual-channel Double Data Rate (DDR) memory architecture supporting PC2700 (333-MHz) and DDR PC3200 (400-MHz). The USDT system provides three DIMM sockets supporting up to 3 GB of memory while all other form factors provide four DIMM sockets and support a total of four gigabytes of memory.

The maximum memory amounts stated above are with 1-GB memory modules using 1-Gb technology DIMMs.

2.4.5 Mass Storage

All models support at least two mass storage devices, with one being externally accessible for removable media. These systems provide one, two, or four SATA interfaces and one PATA interface. These systems may be preconfigured or upgraded with a 40-, 80-, or 160-GB SATA hard drive and one removable media drive such as a CD-ROM drive. Some systems also provide one MultiBay interface.

2.4.6 Serial and Parallel Interfaces

All models except those that use the USDT form factor include a serial port and a parallel port, both of which are accessible at the rear of the chassis. The USDT form factor may be upgraded with an adapter to provide serial and parallel ports. The SFF, ST, MT, and CMT form factors may be upgraded with an optional second serial port.

The serial interface is RS-232-C/16550-compatible and supports standard baud rates up to 115,200 as well as two high-speed baud rates of 230K and 460K. The parallel interface is Enhanced Parallel Port (EPP1.9) and Enhanced Capability Port (ECP) compatible, and supports bi-directional data transfers.

2.4.7 Universal Serial Bus Interface

All models provide eight Universal Serial Bus (USB) ports, with two ports accessible at the front of the unit and six ports accessible on the rear panel. The USB interface provides hot plugging/unplugging functionality. These systems support USB 1.1 and 2.0 functionality on all ports.

2.4.8 Network Interface Controller

All models feature a Broadcom NetXtreme Gigabit Network Interface Controller (NIC) integrated on the system board. The controller provides automatic selection of 10BASE-T, 100BASE-TX, or 1000BASE-T operation with a local area network and includes power-down, wake-up, and Alert-On-LAN (AOL), and Alert Standard Format (ASF) features. An RJ-45 connector with status LEDs is provided on the rear panel.

2.4.9 Graphics Subsystem

These systems use the 82915G or 82915GV GMCH component that integrates an Intel graphics controller that can drive an external VGA monitor. The integrated graphics controller (IGC) features a 333-MHz core processor and a 400-MHz RAMDAC. The controller implements Dynamic Video Memory Technology (DVMT 3.0) for video memory. Table 2-5 lists the key features of the integrated graphics subsystem.

Table 2-5
Integrated Graphics Subsystem Statistics

	82915G or GV GMCH Integrated Graphics Controller
Recommended for:	Hi 2D, Entry 3D
Bus Type	Int. PCI Express
Memory Amount	8 MB pre-allocated
Memory Type	DVMT 3.0
DAC Speed	400 MHz
Maximum 2D Res.	2048x1536 @ 85 Hz
Software Compatibility	Quick Draw, DirectX 9.0, Direct Draw, Direct Show, Open GL 1.4, MPEG 1-2, Indeo
Outputs	1 RGB

The IGC of the 82915G used in the SFF, ST, MT, and CMT form factors supports upgrading through a PCI Express x16 graphics slot. The IGC of the 82915GV used in the USDT form factor does not support a PCI Express x16 graphic slot and may only be upgraded through the PCI 2.3 slot.

2.4.10 Audio Subsystem

These systems use the integrated AC97 audio controller of the chipset and the ADI 1981B audio codec. These systems include microphone and line inputs and headphone and line outputs and include a 3-watt output amplifier driving an internal speaker. All models feature front panel-accessible microphone in and headphone out audio jacks as standard.

2.5 Specifications

This section includes the environmental, electrical, and physical specifications for the systems covered in this guide. Where provided, metric statistics are given in parenthesis. Specifications are subject to change without notice.

Table 2-6
Environmental Specifications (Factory Configuration)

Parameter	Operating	Non-operating
Ambient Air Temperature	50° to 95° F (10° to 35° C, max. rate of change ≤ 10°C/Hr)	-24° to 140° F (-30° to 60° C, max. rate of change ≤ 20°C/Hr)
Shock (w/o damage)	5 Gs [1]	20 Gs [1]
Vibration	0.000215 G^2/Hz, 10-300 Hz	0.0005 G^2/Hz, 10-500 Hz
Humidity	10-90% Rh @ 28° C max. wet bulb temperature	5-95% Rh @ 38.7° C max. wet bulb temperature
Maximum Altitude	10,000 ft (3048 m) [2]	30,000 ft (9144 m) [2]

NOTE:
[1] Peak input acceleration during an 11 ms half-sine shock pulse.
[2] Maximum rate of change: 1500 ft/min.

Table 2-7
Electrical Specifications

Parameter	U.S.	International
Input Line Voltage:		
Nominal:	100–240 VAC	100–240 VAC
Maximum:	90–264 VAC	90–264 VAC
Input Line Frequency Range:		
Nominal:	50–60 Hz	50–60 Hz
Maximum:	47–63 Hz	47–63 Hz
Power Supply:		
Maximum Continuous Power:		
USDT	200 watts	200 watts
ST or SFF	240 watts	240 watts
MT	300 watts [1]	300 watts [1]
CMT	340 watts	340 watts
Maximum Line Current Draw:		
USDT	4 A @ 100 VAC	2 A @ 200 VAC
SF or SFF	5 A @ 100 VAC	2.5 A @ 200 VAC
MT	8 A @ 100 VAC	4 A @ 200 VAC
CMT	6 A @ 100 VAC	3.0 A @ 200 VAC

NOTES:
[1] Some MT SKUs shpped with 340-watt power supplies.

Table 2-8
Physical Specifications

Parameter	USDT	ST	SFF	MT	CMT [3]
Height	2.95 in (7.49 cm)	3.95 in (10.03 cm)	3.95 in (10.03 cm)	14.5 in (36.8 cm)	17.65 in (44.8 cm)
Width	12.4 in (31.5 cm)	13.3 in (33.78 cm)	13.3 in (33.78 cm)	6.88 in 17.5 cm)	6.60 in (16.8 cm)
Depth	13.18 in (33.48 cm)	14.9 in (37.85 cm)	14.9 in (37.85 cm)	16.31 in (41.1 cm)	17.8 in (45.21 cm)
Weight [1]	13.2 lb [2] (6.0 kg) [2]	19.5 lb (8.8 kg)	19.5 lb (8.8 kg)	23.8 lb (10.8 kg)	32.5 lb (14.7 kg)
Load-bearing ability of chassis [4]	100 lb (45.4 kg)	100 lb (45.4 kg)	100 lb (45.4 kg)	n/a	100 lb (45.4 kg)

NOTES:

[1] System weight may vary depending on installed drives/peripherals.

[2] Without MultiBay device installed.

[3] Minitower configuration. For desktop configuration, swap Height and Width dimensions.

[4] Applicable To unit in desktop orientation only and assumes reasonable type of load such as a monitor.

Table 2-9
Diskette Drive Specifications

Parameter	Measurement
Media Type	3.5 in 1.44 MB/720 KB diskette
Height	1/3 bay (1 in)
Bytes per Sector	512
Sectors per Track:	
High Density	18
Low Density	9
Tracks per Side:	
High Density	80
Low Density	80
Read/Write Heads	2
Average Access Time:	
Track-to-Track (high/low)	3 ms/6 ms
Average (high/low)	94 ms/169 ms
Settling Time	15 ms
Latency Average	100 ms

Table 2-10
Optical Drive Specifications

Parameter	48x CD-ROM	48/24/28x CD-RW Drive
Interface Type	IDE	IDE
Media Type (reading)	Mode 1,2, Mixed Mode, CD-DA, Photo CD, Cdi, CD-XA	Mode 1,2, Mixed Mode, CD-DA, Photo CD, Cdi, CD-XA
Media Type (writing)	N/a	CD-R, CD-RW
Transfer Rate (Reads)	4.8 Kb/s (max sustained)	CD-ROM, 4.8 Kb/s; CD-ROM/CD-R, 1.5-6 Kb/s
Transfer Rate (Writes):	N/a	CD-R, 2.4 Kbps (sustained); CD-RW, 1.5 Kbps (sustained);
Capacity:		650 MB @ 12 cm
Mode 1, 12 cm	550 MB	
Mode 2, 12 cm	640 MB	
8 cm	180 MB	
Center Hole Diameter	15 mm	15 mm
Disc Diameter	8/12 cm	8/12 cm
Disc Thickness	1.2 mm	1.2 mm
Track Pitch	1.6 um	1.6 um
Laser		
Beam Divergence	+/- 1.5 °	53.5 + 1.5°
Output Power	0.14 mW	53.6 0.14 mW
Type	GaAs	GaAs
Wave Length	790 +/- 25 nm	790 +/- 25 nm
Average Access Time:		
Random	<100 ms	<120 ms
Full Stroke	<150 ms	<200 ms
Audio Output Level	0.7 Vrms	0.7 Vrms
Cache Buffer	128 KB	128 KB

Table 2-11
Hard Drive Specifications

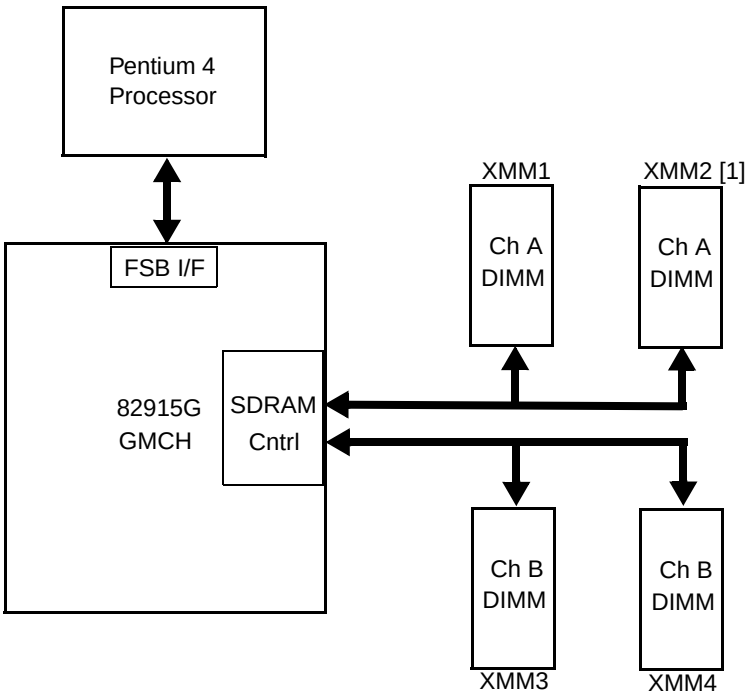
Parameter	40 GB	80 GB	160 GB
Drive Size	3.5 in	3.5 in	3.5 in
Interface	SATA	SATA	SATA
Transfer Rate	150 MB/s	150 MB/s	150 MB/s
Drive Protection System Support?	Yes	Yes	Yes
Typical Seek Time (w/settling)			
Single Track	1.2 ms	0.8 ms	0.8 ms
Average	8.0 ms	9.0 ms	9 ms
Full Stroke	18 ms	17 ms	17 ms
Disk Format (logical blocks)	78,165,360	156,301,488	320,173,056
Rotation Speed	5400/7200	5400/7200	7200 RPM
Drive Fault Prediction	SMART III	SMART III	SMART III

3

Processor/Memory Subsystem

3.1 Introduction

This chapter describes the processor/memory subsystem. These systems feature the Intel Pentium 4 processor and the 915G chipset (Figure 3-1). These systems support PC2700 or PC3200 DDR memory and come standard with PC3200 DIMMs installed.



Note:
[1] SFF, ST, MT, and CMT models only.

Figure 3-1. Processor/Memory Subsystem Architecture

This chapter includes the following topics:

- Pentium 4 processor (3.2), page 3-2
- Memory subsystem (3.3), page 3-4

3.2 Pentium 4 Processor

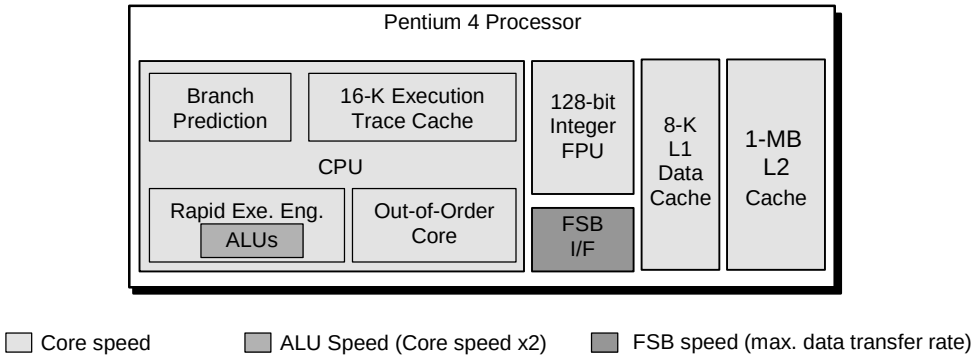
These systems each feature an Intel Pentium 4 processor in a FC-LGA775 package mounted with a passive heat sink in a zero-insertion force socket. The mounting socket allows the processor to be easily changed for servicing and/or upgrading.

3.2.1 Processor Overview

The Intel Pentium 4 processor represents the latest generation of Intel's IA32-class of processors. Featuring Intel's NetBurst architecture and Hyper-Threading technology, the Pentium 4 processor is designed for intensive multimedia and internet applications of today and the future while maintaining compatibility with software written for earlier (Pentium III, Pentium II, Pentium, Celeron, and x86) microprocessors. Key features of the Pentium 4 processor include:

- Hyper-Threading Technology—The main processing loop has twice the depth (20 stages) of earlier processors allowing for increased processing frequencies.
- Execution Trace Cache— A new feature supporting the branch prediction mechanism, the trace cache stores translated sequences of branching micro-operations (ops) and is checked when suspected re-occurring branches are detected in the main processing loop. This feature allows instruction decoding to be removed from the main processing loop.
- Rapid Execution Engine—Arithmetic Logic Units (ALUs) run at twice (2x) processing frequency for higher throughput and reduced latency.
- 1-MB Advanced transfer L2 cache—Using 32-byte-wide interface at processing speed, the large L2 cache provides a substantial increase.
- Advanced dynamic execution—Using a larger (4K) branch target buffer and improved prediction algorithm, branch mis-predictions are reduced by an average of 33 % over the Pentium III.
- Enhanced Floating Point Processor —With 128-bit integer processing and deeper pipelining the Pentium 4's FPU provides a 2x performance boost over the Pentium III.
- Additional Streaming SIMD extensions (SSE2)—In addition to the SSE support provided by previous Pentium processors, the Pentium 4 processor includes an additional 144 MMX instructions, further enhancing:
  - Streaming video/audio processing
  - Photo/video editing
  - Speech recognition
  - 3D processing
  - Encryption processing
- Quad-pumped Front Side Bus (FSB)—The FSB uses a 200-MHz clock for qualifying the buses' control signals. However, address information is transferred using a 2x strobe while data is transferred with a 4x strobe, providing a maximum data transfer rate that is four times that of earlier processors.

Figure 3-2 illustrates the internal architecture of the Intel Pentium 4 processor.



Pentium Type	Core Speed	ALU Speed	FSB Speed	L2 Cache Size
P4 560	3.60 GHz	7.2 GHz	800 MHz	1 MB
P4 550	3.40 GHz	6.8 GHz	800 MHz	1 MB
P4 540	3.20 GHz	6.4 GHz	800 MHz	1 MB
P4 530	3.00 GHz	6.0 GHz	800 MHz	1 MB
P4 520	2.80 GHz	5.6 GHz	800 MHz	1 MB

Figure 3-2. Pentium 4 Processor Internal Architecture

The Intel Pentium 4 increases processing speed by using higher clock speeds with hyper-pipelined technology, therefore handling significantly more instructions at a time. The Pentium 4 features a branch prediction mechanism improved with the addition of an execution trace cache and a refined prediction algorithm. The execution trace cache can store 12 kilobytes of micro-ops (decoded instructions dealing with branching sequences) that are checked when re-occurring branches are processed. Code that is not executed (bypassed) is no longer stored in the L1 cache as was the case in the Pentium III.

The front side bus (FSB) of the Pentium 4 uses a 200-MHz clock but provides bi- and quad-pumped transfers through the use of 2x- and 4x-MHz strobes. The Pentium 4 processor is compatible with software written for x86 processors.

3.2.2 Processor Upgrading

All units use the LGA775 ZIF (Socket T) mounting socket. These systems require that the processor use an integrated heatsink/fan assembly. A replacement processor must use the same type heatsink/fan assembly as the original to ensure proper cooling.

The processor uses a PLGA775 package consisting of the processor die mounted “upside down” on a PC board. This arrangement allows the heat sink to come in direct contact with the processor die. The heat sink and attachment clip are specially designed provide maximum heat transfer from the processor component.

CAUTION: Attachment of the heatsink to the processor is critical on these systems. Improper attachment of the heatsink will likely result in a thermal condition. Although the system is designed to detect thermal conditions and automatically shut down, such a condition could still result in damage to the processor component. Refer to the applicable Service Reference Guide for processor installation instructions.

CAUTION: Installing a processor that is not supported by the system board may cause damage to the system board and/or the processor.

3.3 Memory Subsystem

These systems support PC2700 or PC3200 DDR memory and come standard with PC3200 DIMMs installed.

The DDR SDRAM "PCxxxx" reference designates bus bandwidth (i.e., a PC2700 DIMM can, operating at a 333-MHz effective speed, provide a throughput of 2700 MBps (8 bytes × 333MHz)). Memory speed types may be mixed within a system, although the system BIOS will set the memory controller to work at speed of the slowest DIMM.

The system board provides three or four DIMM sockets depending on form factor:

- XMM1 (black connector), channel A (all form factors
- XMM2 (blue connector), channel A (SFF, ST, MT, and CMT form factors only)
- XMM3 (black connector), channel B (all form factors)
- XMM4 (blue connector), channel B (all form factors)

DIMMs do not need to be installed in pairs although installation of pairs (an equal DIMM for each channel) provides the best performance. The BIOS will detect the DIMM population and set the system accordingly as follows:

- Single-channel mode - DIMMs installed for one channel only
- Dual-channel asymetric mode - DIMMs installed for both channels but of unequal channel capacities.
- Dual-channel interleaved mode (recommended)- DIMMs installed for both channels and offering equal channel capacities, proving the highest performance.

These systems require DIMMs with the following parameters:

- Unbuffered, compatible with SPD rev. 1.0
- 256-Mb, 512-Mb, and 1-Gb memory technology
- x8 and x16 DDR devices
- CAS latency (CL) of 2.5 or 3
- Single or double-sided
- Non-ECC memory only

The SPD format supported by these systems complies with the JEDEC specification for 128-byte EEPROMs. This system also provides support for 256-byte EEPROMs to include additional HP-added features such as part number and serial number. The SPD format as supported in this system (SPD rev. 1) is shown in Table 3-1.

If BIOS detects an unsupported DIMM, a "**memory incompatible**" message will be displayed and the system will halt. **These systems are shipped with non-ECC DIMMs only**. Refer to chapter 8 for a description of the BIOS procedure of interrogating DIMMs.

An installed mix of DIMM types (i.e., PC2700 and PC3200, CL 2 and CL 3) is acceptable but operation will be constrained to the level of the DIMM with the lowest (slowest) performance specification.

If an incompatible DIMM is detected the NUM LOCK will blink for a short period of time during POST and an error message may or may not be displayed before the system hangs.

Table 3-1 shows suggested memory configurations for these systems.

NOTE: Table 3-1 does not list all possible configurations. Balanced-capacity, dual-channel loading yields best performance.

Table 3-1.
DIMM Socket Loading

Channel A		Channel B		
Socket 1	**Socket 2 [1]**	**Socket 3**	**Socket 4**	**Total**
128-MB	none	none	none	128-MB
128-MB	none	128-MB	none	256-MB (dual-channel)
128-MB	128-MB	128-MB	none	384-MB (dual-channel)
128-MB	128-MB	128-MB	128-MB	512-MB (dua- channel)
256-MB	none	none	none	256-MB
256-MB	none	256-MB	none	512-MB (dual-channel)
512-MB	none	none	none	512-MB
512-MB	none	512-MB	none	1-GB (dual-channel)
1-GB	none	none	none	1-GB
1-GB	none	1-GB	none	2-GB (dual-channel)
1-GB	1-GB	1-GB	none	3-GB (dual-channel)
1-GB	1-GB	1-GB	1-GB	4-GB (dual-channel)

NOTE:
[1] SFF. ST, MT, and CMT form factors only.

The SPD address map is shown in Table 3-2.

Table 3-2
SPD Address Map (SDRAM DIMM)

Byte	Description	Notes	Byte	Description	Notes
0	No. of Bytes Written Into EEPROM	[1]	25	Min. CLK Cycle Time at CL X-2	[7]
1	Total Bytes (#) In EEPROM	[2]	26	Max. Acc. Time From CLK @ CL X-2	[7]
2	Memory Type		27	Min. Row Prechge. Time	[7]
3	No. of Row Addresses On DIMM	[3]	28	Min. Row Active to Delay	[7]
4	No. of Column Addresses On DIMM		29	Min. RAS to CAS Delay	[7]
5	No. of Module Banks On DIMM		30-31	Reserved	
6, 7	Data Width of Module		32-61	Superset Data	[7]
8	Voltage Interface Standard of DIMM		62	SPD Revision	[7]
9	Cycletime @ Max CAS Latency (CL)	[4]	63	Checksum Bytes 0-62	
10	Access From Clock	[4]	64-71	JEP-106E ID Code	[8]
11	Config. Type (Parity, Nonparity...)		72	DIMM OEM Location	[8]
12	Refresh Rate/Type	[4][5]	73-90	OEM's Part Number	[8]
13	Width, Primary DRAM		91-92	OEM's Rev. Code	[8]
14	Error Checking Data Width		93-94	Manufacture Date	[8]
15	Min. Clock Delay	[6]	95-98	OEM's Assembly S/N	[8]
16	Burst Lengths Supported		99-125	OEM Specific Data	[8]
17	No. of Banks For Each Mem. Device	[4]	126	Intel frequency check	
18	CAS Latencies Supported	[4]	127	Reserved	
19	CS# Latency	[4]	128 - 131	Compaq header "CPQ1"	[9]
20	Write Latency	[4]	132	Header checksum	[9]
21	DIMM Attributes		133 - 145	Unit serial number	[9][10]
22	Memory Device Attributes		146	DIMM ID	[9][11]
23	Min. CLK Cycle Time at CL X-1	[7]	147	Checksum	[9]
24	Max. Acc. Time From CLK @ CL X-1	[7]	148	Reserved	[9]

NOTES:

[1] Programmed as 128 bytes by the DIMM OEM

[2] Must be programmed to 256 bytes.

[3] High order bit defines redundant addressing: if set (1), highest order RAS# address must be re-sent as highest order CAS# address.

[4] Refer to memory manufacturer's datasheet

[5] MSb is Self Refresh flag. If set (1), assembly supports self refresh.

[6] Back-to-back random column addresses.

[7] Field format proposed to JEDEC but not defined as standard at publication time.

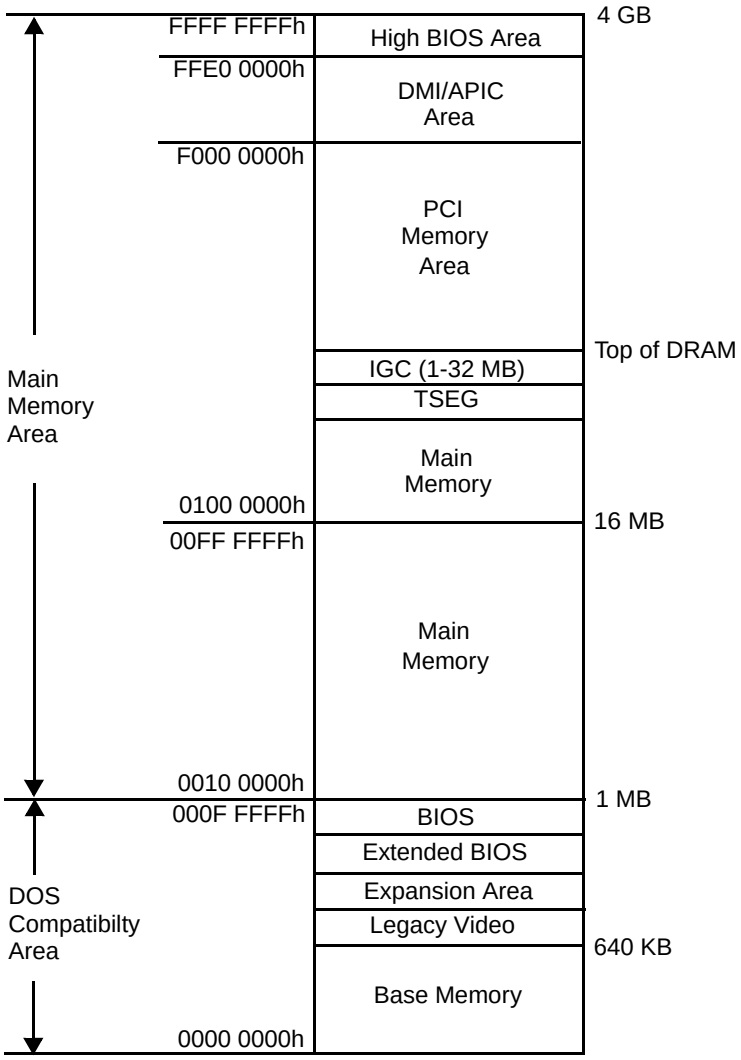
[8] Field specified as optional by JEDEC but required by this system.

[9] HP usage. This system requires that the DIMM EEPROM have this space available for reads/writes.

[10] Serial # in ASCII format (MSB is 133). Intended as backup identifier in case vender data is invalid. Can also be used to indicate s/n mismatch and flag system adminstrator of possible system Tampering.

[11]Contains the socket # of the module (first module is "1"). Intended as backup identifier (refer to note [10]).

Figure 3-3 shows the system memory map.



All locations in memory are cacheable. Base memory is always mapped to DRAM. The next 128 KB fixed memory area can, through the north bridge, be mapped to DRAM or to PCI space. Graphics RAM area is mapped to PCI locations.

Figure 3-3. System Memory Map

4

System Support

4.1 Introduction

This chapter covers subjects dealing with basic system architecture and covers the following topics:

- PCI bus overview (4.2), page 4-1
- System resources (4.3), page 4-11
- Real-time clock and configuration memory (4.4), page 4-19
- System management (4.5), page 4-21
- Register map and miscellaneous functions (4.6), page 4-26

This chapter covers functions provided by off-the-shelf chipsets and therefore describes only basic aspects of these functions as well as information unique to the systems covered in this guide. For detailed information on specific components, refer to the applicable manufacturer's documentation.

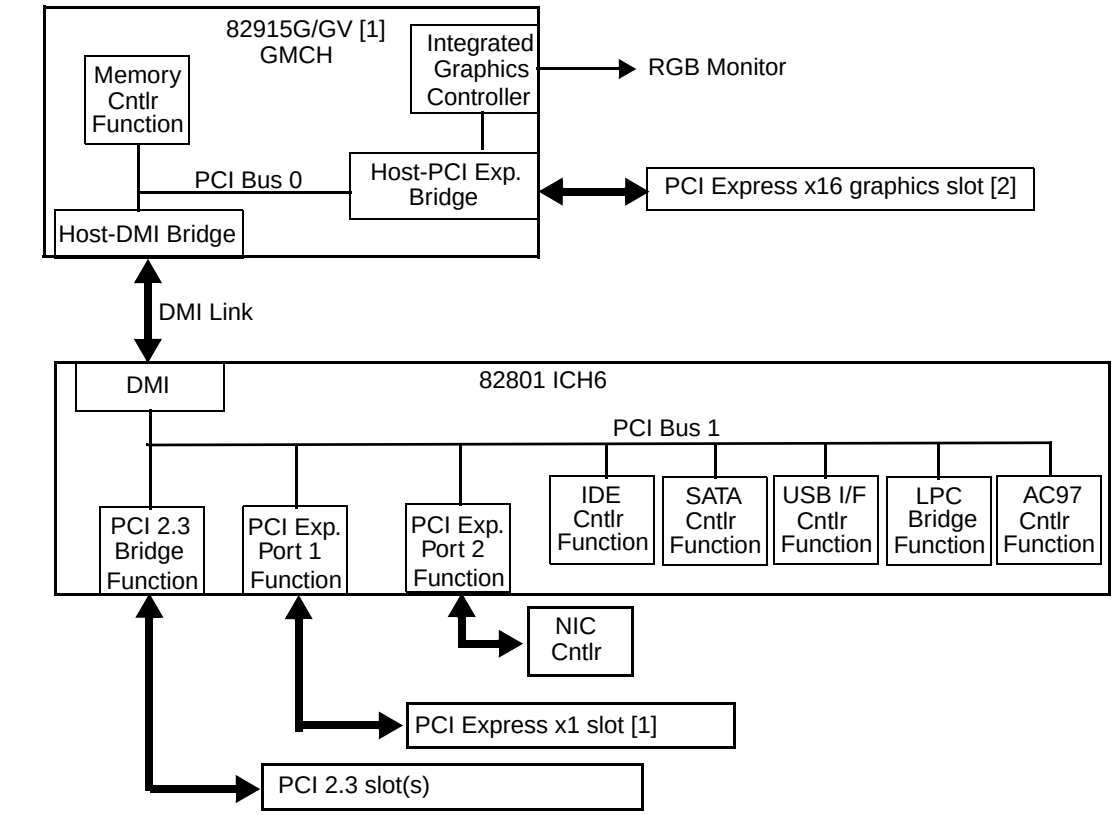
4.2 PCI Bus Overview

This section describes the PCI bus in general and highlights bus implementation in this particular system. For detailed information regarding PCI bus operation, refer to the appropriate PCI specification or the PCI web site: www.pcisig.com.

These systems implement the following types of PCI buses:

- PCI 2.3 - Legacy parallel interface operating at 33-MHz
- PCI Express - High-performance interface capable of using multiple TX/RX high-speed lanes of serial data streams

The PCI bus handles address/data transfers through the identification of devices and functions on the bus. A device is typically defined as a component or slot that resides on the PCI bus (although some components such as the GMCH and ICH6 are organized as multiple devices). A function is defined as the end source or target of the bus transaction. A device may contain one or more functions. In the standard configuration these systems use a hierarchy of three PCI buses (Figure 4-1). The PCI bus #0 is internal to the chipset components and is not physically accessible. The Direct Media Interface (DMI) links the GMCH and ICH6 components and operates as a subset of the PCI bus. All PCI slots and the NIC function internal to the ICH6 reside on PCI bus #2.



Notes:

[1] USDT form factor; 82915GV; SFF, ST, MT, and CMT form factors, 82915G

[2] SFF. ST, MT, and CMT form factors only.

Figure 4-1. PCI Bus Devices and Functions

4.2.1 PCI 2.3 Bus Operation

The PCI 2.3 bus consists of a 32-bit path (AD31-00 lines) that uses a multiplexed scheme for handling both address and data transfers. A bus transaction consists of an address cycle and one or more data cycles, with each cycle requiring a clock (PCICLK) cycle. High performance is realized during burst modes in which a transaction with contiguous memory locations requires that only one address cycle be conducted and subsequent data cycles are completed using auto-incremented addressing. Four types of address cycles can take place on the PCI bus; I/O, memory, configuration, and special. Address decoding is distributed (left up to each device on the PCI bus).

I/O and Memory Cycles

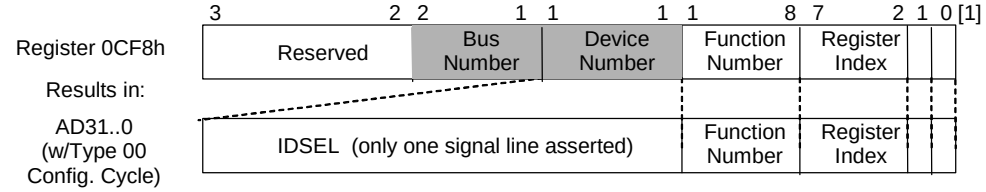
For I/O and memory cycles, a standard 32-bit address decode (AD31..0) for byte-level addressing is handled by the appropriate PCI device. For memory addressing, PCI devices decode the AD31..2 lines for dword-level addressing and check the AD1,0 lines for burst (linear-incrementing) mode. In burst mode, subsequent data phases are conducted a dword at a time with addressing assumed to increment accordingly (four bytes at a time).

Configuration Cycles

Devices on the PCI bus must comply with PCI protocol that allows configuration of that device by software. In this system, configuration mechanism #1 (as described in the PCI Local Bus specification Rev. 2.3) is employed. This method uses two 32-bit registers for initiating a configuration cycle for accessing the configuration space of a PCI device. The configuration address register (CONFIG_ADDRESS) at 0CF8h holds a value that specifies the PCI bus, PCI device, and specific register to be accessed. The configuration data register (CONFIG_DATA) at 0CFCh contains the configuration data.

PCI Configuration Data Register I/O Port 0CFCh, R/W, (8-, 16-, 32-bit access)		**PCI Configuration Address Register I/O Port 0CF8h, R/W, (32-bit access only)**	
Bit	**Function**	**Bit**	**Function**
31	Configuration Enable 0 = Disabled 1 = Enable	31..0	Configuration Data.
30..24	Reserved—read/write 0s		
23..16	Bus Number. Selects PCI bus		
15..11	PCI Device Number. Selects PCI device for access		
10..8	Function Number. Selects function of selected PCI device.		
7..2	Register Index. Specifies config. reg.		
1,0	Configuration Cycle Type ID. 00 = Type 0 01 = Type 1		

Two types of configuration cycles are used. A Type 0 (zero) cycle is targeted to a device on the PCI bus on which the cycle is running. A Type 1 cycle is targeted to a device on a downstream PCI bus as identified by bus number bits <23..16>. With three or more PCI buses, a PCI bridge may convert a Type 1 to a Type 0 if it's destined for a device being serviced by that bridge or it may forward the Type 1 cycle unmodified if it is destined for a device being serviced by a downstream bridge. Figure 4-2 shows the configuration cycle format and how the loading of 0CF8h results in a Type 0 configuration cycle on the PCI bus. The Device Number (bits <15..11> determines which one of the AD31..11 lines is to be asserted high for the IDSEL signal, which acts as a “chip select” function for the PCI device to be configured. The function number (CF8h, bits <10..8>) is used to select a particular function within a PCI component.



NOTES:

[1] Bits <1,0> : 00 = Type 0 Cycle, 01 = Type 1 cycle
Type 01 cycle only. Reserved on Type 00 cycle.

Figure 4-2. Configuration Cycle

Table 4-1 shows the standard configuration of device numbers and IDSEL connections for components and slots residing on a PCI 2.3 bus.

Table 4-1
PCI Component Configuration Access

PCI Component	Notes	Function #	Device #	PCI Bus #	IDSEL Wired to:
82915G GMCH:					--
Host/DMI Bridge		0	28	0	
Host/PCI Expr. Bridge		1	28	0	
Integrated Graphics Cntlr.		0	2	0	
PCI Express x16 graphics slot [1]		0	0	32	--
82801EB ICH6					--
PCI Bridge		0	30	0	
LPC Bridge		0	31	0	
IDE Controller		1	31	0	
Serial ATA Controller		2	31	0	
SMBus Controller		3	31	0	
USB I/F #1		0	29	0	
USB I/F #2		1	29	0	
USB I/F #3		2	29	0	
USB I/F #4		3	29	0	
USB 2.0 Controller		7	29	0	
AC97 Audio Controller		2	30	0	
AC97 Modem Controller	[1]	3	30	0	
Network Interface Controller	[1]	0	0	64	
PCI Express port 1		0	28	0	
PCI Express port 2		1	28	0	
PCI 2.3 slot 1		0	4	8	AD20
PCI 2.3 slot 2	[2]	0	9	8	AD25
PCI 2.3 slot 3	[3]	0	10	8	AD27
PCI 2.3 slot 4	[3]	0	11	8	AD29

NOTES:

[1] Not used in these systems.

[2] SFF, ST, MT, & CMT form factors only.

[3] CMT form factor with PCI expansion board.

The register index (CF8h, bits <7..2>) identifies the 32-bit location within the configuration space of the PCI device to be accessed. All PCI devices can contain up to 256 bytes of configuration data (Figure 4-3), of which the first 64 bytes comprise the configuration space header.

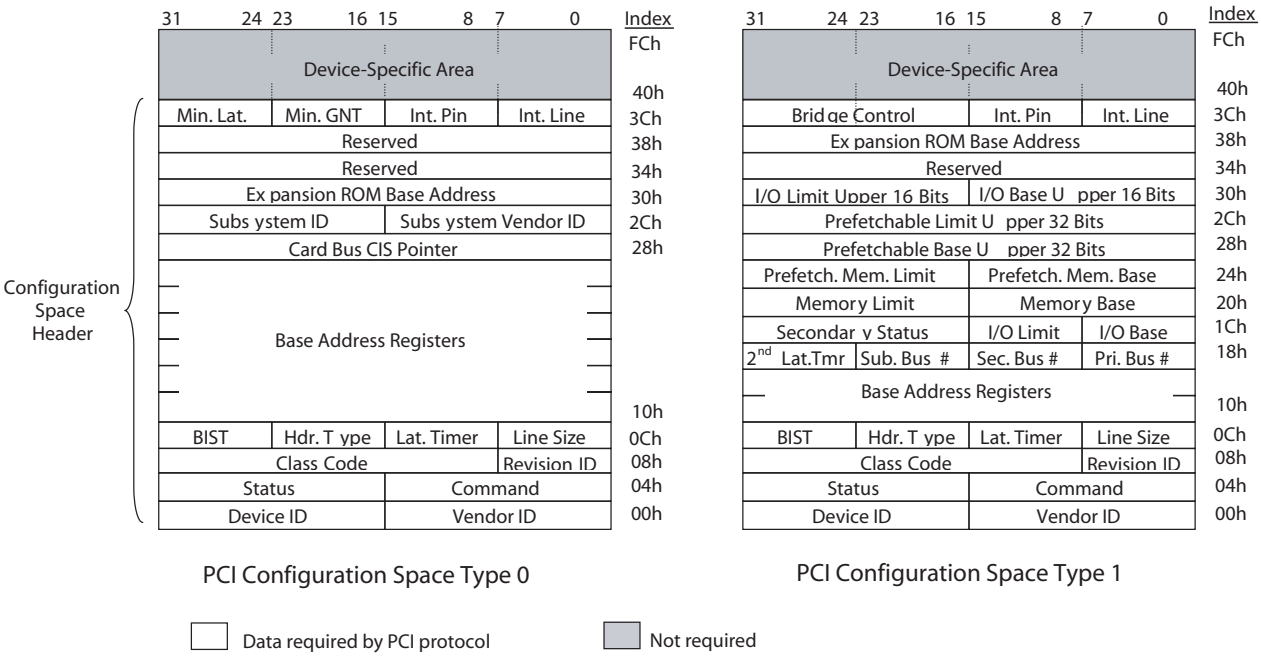


Figure 4-3. PCI Configuration Space Mapping

PCI 2.3 Bus Master Arbitration

The PCI bus supports a bus master/target arbitration scheme. A bus master is a device that has been granted control of the bus for the purpose of initiating a transaction. A target is a device that is the recipient of a transaction. The Request (REQ), Grant (GNT), and FRAME signals are used by PCI bus masters for gaining access to the PCI bus. When a PCI device needs access to the PCI bus (and does not already own it), the PCI device asserts it's REQn signal to the PCI bus arbiter (a function of the system controller component). If the bus is available, the arbiter asserts the GNTn signal to the requesting device, which then asserts FRAME and conducts the address phase of the transaction with a target. If the PCI device already owns the bus, a request is not needed and the device can simply assert FRAME and conduct the transaction. Table 4-3 shows the grant and request signals assignments for the devices on the PCI bus.

Table 4-3.
PCI Bus Mastering Devices

Device	REQ/GNT Line	Note
PCI Connector Slot 1	REQ0/GNT0	
PCI Connector Slot 2	REQ1/GNT1	[1]
PCI Connector Slot 3	REQ2/GNT2	[2]
PCI Connector Slot 4	REQ3/GNT3	[2]

NOTE:

[1]SFF, ST, MT, and CMT form factors only.

[2] CMT form factor with PCI expansion board

PCI bus arbitration is based on a round-robin scheme that complies with the fairness algorithm specified by the PCI specification. The bus parking policy allows for the current PCI bus owner (excepting the PCI/ISA bridge) to maintain ownership of the bus as long as no request is asserted by another agent. Note that most CPU-to-DRAM and PCI-E-to-DRAM accesses can occur concurrently with PCI traffic, therefore reducing the need for the Host/PCI bridge to compete for PCI bus ownership.

4.2.2 PCI Express Bus Operation

The PCI Express bus is a high-performace extension of the legacy PCI bus specification. The PCI Express bus uses the following layers:

- Software/driver layer
- Transaction protocol layer
- Link layer
- Physical layer

Software/Driver Layer

The PCI Express bus maintains software compatibility with PCI 2.3 and earlier versions so that there is no impact on existing operating systems and drivers. During system intialization, the PCI Express bus uses the same methods of device discovery and resource allocation that legacy PCI-based operating systems and drivers are designed to use. The use of PCI configuration space and the programmability of I/O devices are also used in the same way as for legacy PCI buses. The software/driver layer provides read and write requests to the transaction layer for handling a data transfer.

Transaction Protocol Layer

The transaction protocol layer processes read and write requests from the software/driver layer and generates request packets for the link layer. Each packet includes an identifier allowing any required responcse packets to be directed to the originator.

PCI Express protocol supports the three legacy PCI address spaces (memory, I/O, configuration) as well as a new message space. The message space allows in-band processing of interrupts through use of the Message Signal Interrupt (MSI) introduced with the PCI 2.2 specification. The MSI method eliminates the need for hard-wired sideband signals by incorporating those functions into packets.

Link Layer

The link layer provides data integrity by adding a sequence information prefix and a CRC suffix to the packet created by the transaction layer. Flow-control methods ensure that a packet will only be transferred if the receiving device is ready to accomodate it. A corrupted packet will be automatically re-sent.

Physical Layer

The PCI Express bus uses a point-to-point, high-speed TX/RX serial lane topology. that can be scalable as to the the end point's requirements. One or more full-duplex lanes transfer data serially. Each lane consists of two differential pairs of signal paths (Figure 4-4), one for transmit, one for receive.

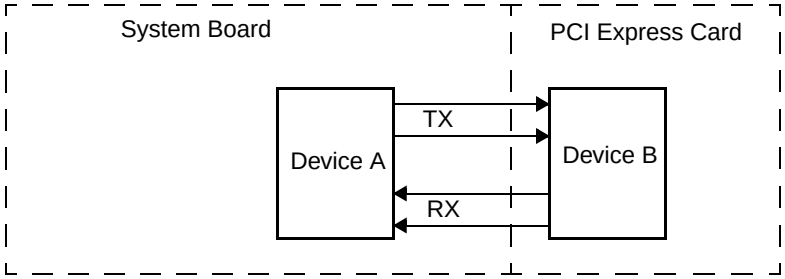


Figure 4-4. PCI Express Bus Lane

Each byte is transferred using 8b/10b encoding. which embeds the clock signal with the data. Operating at a 2.5 Gigabit transfer rate, a single lane can provide a data flow of 200 MBps. The bandwidth is increased if additional lanes are available for use. During the initialization process, two PCI Express devices will negotiate for the number of lanes available and the speed the link can operate at.

In a x1 (single lane) interface, all data bytes are transferred serially over the lane. In a multi-lane interface, data bytes are distributed across the lanes using a multiplex scheme as shown in Table 4-4:

Table 4-4.
PCI Express Byte Transfer

Byte #	x1 Transfer Lane #	x4 Transfer Lane #	x8 Transfer Lane #
0	0	0	0
1	0	1	1
2	0	2	2
3	0	3	3
4	0	0	4
5	0	1	5
6	0	2	6
7	0	3	7

For a PCI Express x16 transfer, a lane will be re-used every17th byte of a transfer. The mux-demux process provided by the physical layer is transparent to the other layers and to software/drivers.

The SFF, ST, MT MT, and CMT forma factors provide two PCI Express slots: a PCI Express x16 (16-lane) slot specifically designed for a graphics controller, and a general purpose PCI Express x1 (1-lane) slot.

4.2.3 Option ROM Mapping

During POST, the PCI bus is scanned for devices that contain their own specific firmware in ROM. Such option ROM data, if detected, is loaded into system memory's DOS compatibility area (refer to the system memory map shown in chapter 3).

4.2.4 PCI Interrupts

Eight interrupt signals (INTA- thru INTH-) are available for use by PCI devices. These signals may be generated by on-board PCI devices or by devices installed in the PCI slots. For more information on interrupts including PCI interrupt mapping refer to the “System Resources” section 4.3.

4.2.5 PCI Power Management Support

This system complies with the PCI Power Management Interface Specification (rev 1.0). The PCI Power Management Enable (PME-) signal is supported by the chipset and allows compliant PCI peripherals to initiate the power management routine.

4.2.6 PCI Connectors

PCI 2.3 Connector

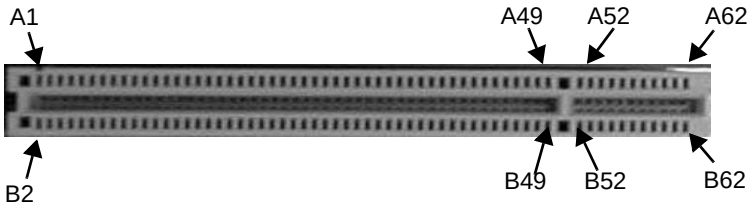


Figure 4-5. PCI 2.3 Bus Connector (32-Bit, 5.0-volt Type)

Table 4-5.
PCI 2.3 Bus Connector Pinout

Pin	B Signal	A Signal	Pin	B Signal	A Signal	Pin	B Signal	A Signal
01	-12 VDC	TRST-	22	GND	AD28	43	+3.3 VDC	PAR
02	TCK	+12 VDC	23	AD27	AD26	44	C/BE1-	AD15
03	GND	TMS	24	AD25	GND	45	AD14	+3.3 VDC
04	TDO	TDI	25	+3.3 VDC	AD24	46	GND	AD13
05	+5 VDC	+5 VDC	26	C/BE3-	IDSEL	47	AD12	AD11
06	+5 VDC	INTA-	27	AD23	+3.3 VDC	48	AD10	GND
07	INTB-	INTC-	28	GND	AD22	49	GND	AD09
08	INTD-	+5 VDC	29	AD21	AD20	50	Key	Key
09	PRSNT1-	Reserved	30	AD19	GND	51	Key	Key
10	RSVD	+5 VDC	31	+3.3 VDC	AD18	52	AD08	C/BE0-
11	PRSNT2-	Reserved	32	AD17	AD16	53	AD07	+3.3 VDC
12	GND	GND	33	C/BE2-	+3.3 VDC	54	+3.3 VDC	AD06
13	GND	GND	34	GND	FRAME-	55	AD05	AD04
14	RSVD	+3.3 AUX	35	IRDY-	GND	56	AD03	GND
15	GND	RST-	36	+3.3 VDC	TRDY-	57	GND	AD02
16	CLK	+5 VDC	37	DEVSEL-	GND	58	AD01	AD00
17	GND	GNT-	38	GND	STOP-	59	+5 VDC	+5 VDC
18	REQ-	GND	39	LOCK-	+3.3 VDC	60	ACK64-	REQ64-
19	+5 VDC	PME-	40	PERR-	SDONE n	61	+5 VDC	+5 VDC
20	AD31	AD30	41	+3.3 VDC	SBO-	62	+5 VDC	+5 VDC
21	AD29	+3.3 VDC	42	SERR-	GND			

PCI Express Connectors

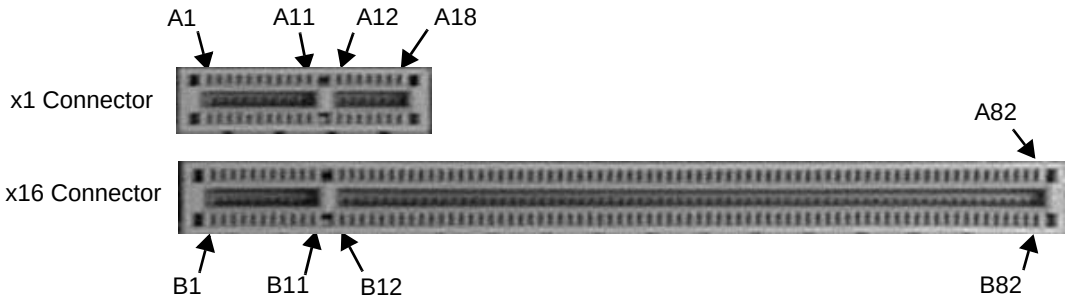


Figure 4-6. PCI Express Bus Connectors

Table 4-6.
PCI Express Bus Connector Pinout

Pin	B Signal	A Signal	Pin	B Signal	A Signal	Pin	B Signal	A Signal
01	+12 VDC	PRSNT1#	29	GND	PERp3	57	GND	PERn9
02	+12 VDC	+12 VDC	30	RSVD	PERn3	58	PETp10	GND
03	RSVD	+12 VDC	31	PRSNT2#	GND	59	PETn10	GND
04	GND	GND	32	GND	RSVD	60	GND	PERp10
05	SMCLK	+5 VDC	33	PETp4	RSVD	61	GND	PERn10
06	+5 VDC	JTAG2	34	PETn4	GND	62	PETp11	GND
07	GND	JTAG4	35	GND	PERp4	63	PETn11	GND
08	+3.3 VDC	JTAG5	36	GND	PERn4	64	GND	PERp11
09	JTAG1	+3.3 VDC	37	PETp5	GND	65	GND	PERn11
10	3.3 Vaux	+3.3 VDC	38	PETn5	GND	66	PETp12	GND
11	WAKE	PERST#	39	GND	PERp5	67	PETn12	GND
12	RSVD	GND	40	GND	PERn5	68	GND	PERp12
13	GND	REFCLK+	41	PETp6	GND	69	GND	PERn12
14	PETp0	REFCLK-	42	PETn6	GND	70	PETp13	GND
15	PETn0	GND	43	GND	PERp6	71	PETn13	GND
16	GND	PERp0	44	GND	PERn6	72	GND	PERp13
17	PRSNT2#	PERn0	45	PETp7	GND	73	GND	PERn13
18	GND	GND	46	PETn7	GND	74	PETp14	GND
19	PETp1	RSVD	47	GND	PERp7	75	PETn14	GND
20	PETn1	GND	48	PRSNT2#	PERn7	76	GND	PERp14
21	GND	PERp1	49	GND	GND	77	GND	PERn14
22	GND	PERn1	50	PETp8	RSVD	78	PETp15	GND
23	PETp2	GND	51	PETn8	GND	79	PETn15	GND
24	PETn2	GND	52	GND	PERp8	80	GND	PERp15
25	GND	PERp2	53	GND	PERn8	81	PRSNT2#	PERn15
26	GND	PERn2	54	PETp9	GND	82	RSVD	GND
27	PETp3	GND	55	PETn9	GND			
28	PETn3	GND	56	GND	PERp9			

4.3 System Resources

This section describes the availability and basic control of major subsystems, otherwise known as resource allocation or simply “system resources.” System resources are provided on a priority basis through hardware interrupts and DMA requests and grants.

4.3.1 Interrupts

The microprocessor uses two types of hardware interrupts; maskable and nonmaskable. A maskable interrupt can be enabled or disabled within the microprocessor by the use of the STI and CLI instructions. A nonmaskable interrupt cannot be masked off within the microprocessor, although it may be inhibited by hardware or software means external to the microprocessor.

Maskable Interrupts

The maskable interrupt is a hardware-generated signal used by peripheral functions within the system to get the attention of the microprocessor. Peripheral functions produce a unique INTA-H (PCI) or IRQ0-15 (ISA) signal that is routed to interrupt processing logic that asserts the interrupt (INTR-) input to the microprocessor. The microprocessor halts execution to determine the source of the interrupt and then services the peripheral as appropriate.

Most IRQs are routed through the I/O controller of the super I/O component, which provides the serializing function. A serialized interrupt stream is then routed to the ICH component.

Interrupts may be processed in one of two modes (selectable through the F10 Setup utility):

- 8259 mode
- APIC mode

These modes are described in the following subsections.

8259 Mode

The 8259 mode handles interrupts IRQ0-IRQ15 in the legacy (AT-system) method using 8259-equivalent logic. Table 4-7 lists the standard source configuration for maskable interrupts and their priorities in 8259 mode. If more than one interrupt is pending, the highest priority (lowest number) is processed first.

Table 4-7.
Maskable Interrupt Priorities and Assignments

Priority	Signal Label	Source (Typical)
1	IRQ0	Interval timer 1, counter 0
2	IRQ1	Keyboard
3	IRQ8-	Real-time clock
4	IRQ9	Unused
5	IRQ10	PCI devices/slots
6	IRQ11	Audio codec
7	IRQ12	Mouse
8	IRQ13	Coprocessor (math)
9	IRQ14	Primary IDE controller
10	IRQ15	Sec. IDE I/F controller (not available on SATA units)
11	IRQ3	Serial port (COM2)
12	IRQ4	Serial port (COM1)
13	IRQ5	Network interface controller
14	IRQ6	Diskette drive controller
15	IRQ7	Parallel port (LPT1)
–	IRQ2	NOT AVAILABLE (Cascade from interrupt controller 2)

APIC Mode

The Advanced Programmable Interrupt Controller (APIC) mode provides enhanced interrupt processing with the following advantages:

- Eliminates the processor's interrupt acknowledge cycle by using a separate (APIC) bus
- Programmable interrupt priority
- Additional interrupts (total of 24)

The APIC mode accommodates eight PCI interrupt signals (INTA-..INTH-) for use by PCI devices. The PCI interrupts are evenly distributed to minimize latency and wired as follows:

		PCI_ Slot 1	PCI Slot 2	PCI Slot 3	PCI_ Slot 4
INTA-	Wired to	INTA-	INTD-	INTB-	INTD-
INTB-		—	—	—	—
INTC-		INTB-	INTA-	INTC-	INTA-
INTD-		—	—	—	—
INTE-		—	—	—	—
INTF-		INTC-	INTB-	INTD-	INTB-
INTG-		INTD-	INTC-	INTA-	INTC-
INTH-		—	—	—	—

NOTES:

[1] Connection internal to the ICH. Will be reported by BIOS as using INTA but is NOT shared with other functions using INTA.

MT, CMT form factors only.

SFF, ST, MT, CMT form factors only.

The PCI interrupts can be configured by PCI Configuration Registers 60h..63h to share the standard ISA interrupts (IRQn).

The APIC mode is supported by the Windows NT, Windows 2000, and Windows XP operating systems. Systems running the Windows 95 or 98 operating system will need to run in 8259 mode.

Maskable Interrupt processing is controlled and monitored through standard AT-type I/O-mapped registers. These registers are listed in Table 4-8.

Table 4-8.
Maskable Interrupt Control Registers

I/O Port	Register
020h	Base Address, Int. Cntlr. 1
021h	Initialization Command Word 2-4, Int. Cntlr. 1
0A0h	Base Address, Int. Cntlr. 2
0A1h	Initialization Command Word 2-4, Int. Cntlr. 2

The initialization and operation of the interrupt control registers follows standard AT-type protocol.

Non-Maskable Interrupts

Non-maskable interrupts cannot be masked (inhibited) within the microprocessor itself but may be maskable by software using logic external to the microprocessor. There are two non-maskable interrupt signals: the NMI- and the SMI-. These signals have service priority over all maskable interrupts, with the SMI- having top priority over all interrupts including the NMI-.

NMI- Generation

The Non-Maskable Interrupt (NMI-) signal can be generated by one of the following actions:

- Parity errors detected on a PCI bus (activating SERR- or PERR-).
- Microprocessor internal error (activating IERRA or IERRB)

The SERR- and PERR- signals are routed through the ICH6 component, which in turn activates the NMI to the microprocessor.

The NMI Status Register at I/O port 061h contains NMI source and status data as follows:

NMI Status Register 61h

Bit	Function
7	NMI Status: 0 = No NMI from system board parity error. 1 = NMI requested, read only
6	IOCHK- NMI: 0 = No NMI from IOCHK- 1 = IOCHK- is active (low), NMI requested, read only
5	Interval Timer 1, Counter 2 (Speaker) Status
4	Refresh Indicator (toggles with every refresh)
3	IOCHK- NMI Enable/Disable: 0 = NMI from IOCHK- enabled 1 = NMI from IOCHK- disabled and cleared (R/W)
2	System Board Parity Error (PERR/SERR) NMI Enable: 0 = Parity error NMI enabled 1 = Parity error NMI disabled and cleared (R/W)
1	Speaker Data (R/W)
0	Inteval Timer 1, Counter 2 Gate Signal (R/W) 0 = Counter 2 disabled 1 = Counter 2 enabled

Functions not related to NMI activity

After the active NMI has been processed, status bits <7> or <6> are cleared by pulsing bits <2> or <3> respectively.

The NMI Enable Register (070h, <7>) is used to enable/disable the NMI signal. Writing 80h to this register masks generation of the NMI-. Note that the lower six bits of register at I/O port 70h affect RTC operation and should be considered when changing NMI- generation status.

SMI- Generation

The SMI- (System Management Interrupt) is typically used for power management functions. When power management is enabled, inactivity timers are monitored. When a timer times out, SMI- is asserted and invokes the microprocessor's SMI handler. The SMI- handler works with the APM BIOS to service the SMI- according to the cause of the timeout.

Although the SMI- is primarily used for power management the interrupt is also employed for the QuickLock/QuickBlank functions as well.

4.3.2 Direct Memory Access

Direct Memory Access (DMA) is a method by which a device accesses system memory without involving the microprocessor. Although the DMA method has been traditionally used to transfer blocks of data to or from an ISA I/O device, PCI devices may also use DMA operation as well. The DMA method reduces the amount of CPU interactions with memory, freeing the CPU for other processing tasks.

This section describes DMA in general. For detailed information regarding DMA operation, refer to the data manual for the Intel 82801 I/O Controller Hub.

The 82801 ICH6 component includes the equivalent of two 8237 DMA controllers cascaded together to provide eight DMA channels, each (excepting channel 4) configurable to a specific device. Table 4-9 lists the default configuration of the DMA channels.

Table 4-9.
Default DMA Channel Assignments

DMA Channel	Device ID
Controller 1 (byte transfers)	
0	Spare
1	Audio subsystem
2	Diskette drive
3	Parallel port
Controller 2 (word transfers)	
4	Cascade for controller 1
5	Spare
6	Spare
7	Spare

All channels in DMA controller 1 operate at a higher priority than those in controller 2. Note that channel 4 is not available for use other than its cascading function for controller 1. The DMA controller 2 can transfer words only on an even address boundary. The DMA controller and page register define a 24-bit address that allows data transfers within the address space of the CPU.

In addition to device configuration, each channel can be configured (through PCI Configuration Registers) for one of two modes of operation:

- LPC DMA
- PC/PCI DMA

The LPC DMA mode uses the LPC bus to communicate DMA channel control and is implemented for devices using DMA through the LPC47B397 I/O controller such as the diskette drive controller.

The PC/PCI DMA mode uses the REQ#/GNT# signals to communicate DMA channel control and is used by PCI expansion devices.

The DMA logic is accessed through two types of I/O mapped registers; page registers and controller registers.

DMA Page Registers

The DMA page register contains the eight most significant bits of the 24-bit address and works in conjunction with the DMA controllers to define the complete (24-bit) address for the DMA channels. Table 4-10 lists the page register port addresses.

Table 4-10.
DMA Page Register Addresses

DMA Channel	Page Register I/O Port
Controller 1 (byte transfers)	
Ch 0	087h
Ch 1	083h
Ch 2	081h
Ch 3	082h
Controller 2 (word transfers)	
Ch 4	n/a
Ch 5	08Bh
Ch 6	089h
Ch 7	08Ah
Refresh	08Fh [see note]

NOTE:

The DMA memory page register for the refresh channel must be programmed with 00h for proper operation.

The memory address is derived as follows:

24-Bit Address—Controller 1 (Byte Transfers)	
8-Bit Page Register	8-Bit DMA Controller
A23..A16	A15..A00

24-Bit Address—Controller 2 (Word Transfers)	
8-Bit Page Register	16-Bit DMA Controller
A23..A17	A16..A01, (A00 = 0)

Note that address line A16 from the DMA memory page register is disabled when DMA controller 2 is selected. Address line A00 is not connected to DMA controller 2 and is always 0 when word-length transfers are selected.

By not connecting A00, the following applies:

- The size of the the block of data that can be moved or addressed is measured in 16-bits (words) rather than 8-bits (bytes).
- The words must always be addressed on an even boundary.

DMA controller 1 can move up to 64 Kbytes of data per DMA transfer. DMA controller 2 can move up to 64 Kwords (128 Kbytes) of data per DMA transfer. Word DMA operations are only possible between 16-bit memory and 16-bit peripherals.

The RAM refresh is designed to perform a memory read cycle on each of the 512 row addresses in the DRAM memory space. Refresh operations are used to refresh memory on the 32-bit memory bus and the ISA bus. The refresh address is provided on lines SA00 through SA08. Address lines LA23..17, SA18,19 are driven low.

The remaining address lines are in an undefined state during the refresh cycle. The refresh operations are driven by a 69.799-KHz clock generated by Interval Timer 1, Counter 1. The refresh rate is 128 refresh cycles in 2.038 ms.

DMA Controller Registers

Table 4-11 lists the DMA Controller Registers and their I/O port addresses. Note that there is a set of registers for each DMA controller.

Table 4-11.
DMA Controller Registers

Register	Controller 1	Controller 2	R/W
Status	008h	0D0h	R
Command	008h	0D0h	W
Mode	00Bh	0D6h	W
Write Single Mask Bit	00Ah	0D4h	W
Write All Mask Bits	00Fh	0DEh	W
Software DRQx Request	009h	0D2h	W
Base and Current Address—Ch 0	000h	0C0h	W
Current Address—Ch 0	000h	0C0h	R
Base and Current Word Count—Ch 0	001h	0C2h	W
Current Word Count—Ch 0	001h	0C2h	R
Base and Current Address—Ch 1	002h	0C4h	W
Current Address—Ch 1	002h	0C4h	R
Base and Current Word Count—Ch 1	003h	0C6h	W
Current Word Count—Ch 1	003h	0C6h	R
Base and Current Address—Ch 2	004h	0C8h	W
Current Address—Ch 2	004h	0C8h	R
Base and Current Word Count—Ch 2	005h	0CAh	W
Current Word Count—Ch 2	005h	0CAh	R
Base and Current Address—Ch 3	006h	0CCh	W
Current Address—Ch 3	006h	0CCh	R
Base and Current Word Count—Ch 3	007h	0CEh	W
Current Word Count—Ch 3	007h	0CEh	R
Temporary (Command)	00Dh	0DAh	R
Reset Pointer Flip-Flop (Command)	00Ch	0D8h	W
Master Reset (Command)	00Dh	0DAh	W
Reset Mask Register (Command)	00Eh	0DCh	W

4.4 Real-Time Clock and Configuration Memory

The Real-time clock (RTC) and configuration memory (also referred to as “CMOS”) functions are provided by the 82801 component and is MC146818-compatible. As shown in the following figure, the 82801 ICH6 component provides 256 bytes of battery-backed RAM divided into two 128-byte configuration memory areas. The RTC uses the first 14 bytes (00-0Dh) of the standard memory area. All locations of the standard memory area (00-7Fh) can be directly accessed using conventional OUT and IN assembly language instructions through I/O ports 70h/71h, although the suggested method is to use the INT15 AX=E823h BIOS call.

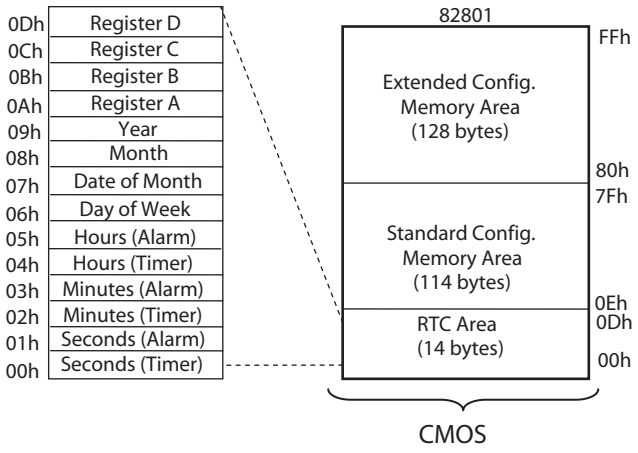


Figure 4 11. Configuration Memory Map

A lithium 3-VDC battery is used for maintaining the RTC and configuration memory while the system is powered down. During system operation a wire-Ored circuit allows the RTC and configuration memory to draw power from the power supply. The battery is located in a battery holder on the system board and has a life expectancy of four to eight years. When the battery has expired it is replaced with a Renata CR2032 or equivalent 3-VDC lithium battery.

4.4.1 Clearing CMOS

The contents of configuration memory (including the Power-On Password) can be cleared by the following procedure:

1. Turn off the unit.
2. Disconnect the AC power cord from the outlet and/or system unit.
3. Remove the chassis hood (cover) and insure that no LEDs on the system board are illuminated.
4. On the system board, press and hold the CMOS clear button for at least 5 seconds.
5. Replace the chassis hood (cover).
6. Reconnect the AC power cord to the outlet and/or system unit.
7. Turn the unit on.

To clear only the Power-On Password refer to section 4.5.1.

4.4.2 CMOS Archive and Restore

During the boot sequence the BIOS saves a copy of NVRAM (CMOS contents, password(s) and other system variables) in a portion of the flash ROM. Should the system become un-usable, the last good copy of NVRAM data can be restored with the Power Button Override function. This function is invoked with the following procedure:

1. With the unit powered down, press and release the power button.
2. Immediately after releasing the power button in step 1, press and hold the power button until the unit powers down. This action will be recorded as a Power Button Override event.

With the next startup sequence the BIOS will detect the occurrence of the Power Button Override event and will load the backup copy of NVRAM from the ROM to the CMOS.

The Power Button Override feature does not allow quick cycling of the system (turning on then off). If the power cord is disconnected during the POST routine, the splash screen image may become corrupted, requiring a re-flashing of the ROM (refer to chapter 8, BIOS ROM).

4.4.3 Standard CMOS Locations

Table 4-12 describes standard configuration memory locations 0Ah-3Fh. These locations are accessible through using OUT/IN assembly language instructions using port 70/71h or BIOS function INT15, AX=E823h.

Table 4-12.
Configuration Memory (CMOS) Map

Location	Function	Location	Function
00-0Dh	Real-time clock	24h	System board ID
0Eh	Diagnostic status	25h	System architecture data
0Fh	System reset code	26h	Auxiliary peripheral configuration
10h	Diskette drive type	27h	Speed control external drive
11h	Reserved	28h	Expanded/base mem. size, IRQ12
12h	Hard drive type	29h	Miscellaneous configuration
13h	Security functions	2Ah	Hard drive timeout
14h	Equipment installed	2Bh	System inactivity timeout
15h	Base memory size, low byte/KB	2Ch	Monitor timeout, Num Lock Cntrl
16h	Base memory size, high byte/KB	2Dh	Additional flags
17h	Extended memory, low byte/KB	2Eh-2Fh	Checksum of locations 10h-2Dh
18h	Extended memory, high byte/KB	30h-31h	Total extended memory tested
19h	Hard drive 1, primary controller	32h	Century
1Ah	Hard drive 2, primary controller	33h	Miscellaneous flags set by BIOS
1Bh	Hard drive 1, secondary controller	34h	International language
1Ch	Hard drive 2, secondary controller	35h	APM status flags
1Dh	Enhanced hard drive support	36h	ECC POST test single bit
1Eh	Reserved	37h-3Fh	Power-on password
1Fh	Power management functions	40-FFh	Feature Control/Status

NOTES:

Assume unmarked gaps are reserved.

Higher locations (>3Fh) contain information that should be accessed using the INT15, AX=E845h BIOS function (refer to Chapter 8 for BIOS function descriptions).

4.5 System Management

This section describes functions having to do with security, power management, temperature, and overall status. These functions are handled by hardware and firmware (BIOS) and generally configured through the Setup utility.

4.5.1 Security Functions

These systems include various features that provide different levels of security. Note that this subsection describes only the hardware functionality (including that supported by Setup) and does not describe security features that may be provided by the operating system and application software.

Power-On / Setup Password

These systems include a power-on and setup passwords, which may be enabled or disabled (cleared) through a jumper on the system board. The jumper controls a GPIO input to the 82801 ICH6 that is checked during POST. The password is stored in configuration memory (CMOS) and if enabled and then forgotten by the user will require that either the password be cleared (preferable solution and described below) or the entire CMOS be cleared (refer to section 4.4.1).

To clear the password, use the following procedure:

1. Turn off the system and disconnect the AC power cord from the outlet and/or system unit.
2. Remove the cover (hood) as described in the appropriate User Guide or Maintainance And Service Reference Guide. Insure that all system board LEDs are off (not illuminated).
3. Locate the password clear jumper (header is labeled E49 on these systems) and move the jumper from pins 1 and 2 and place on (just) pin 2 (for safekeeping).
4. Replace the cover.
5. Re-connect the AC power cord to the AC outlet and/or system unit.
6. Turn on the system. The POST routine will clear and disable the password.
7. To re-enable the password feature, repeat steps 1-6, replacing the jumper on pins 1 and 2 of header E49.

Setup Password

The Setup utility may be configured to be always changeable or changeable only by entering a password. Refer to the previous procedure (Power On / Setup Password) for clearing the Setup password.

Cable Lock Provision

These systems include a chassis cutout (on the rear panel) for the attachment of a cable lock mechanism.

I/O Interface Security

The serial, parallel, USB, and diskette interfaces may be disabled individually through the Setup utility to guard against unauthorized access to a system. In addition, the ability to write to or boot from a removable media drive (such as the diskette drive) may be enabled through the Setup utility. The disabling of the serial, parallel, and diskette interfaces are a function of the LPC47B397 I/O controller. The USB ports are controlled through the 82801.

Chassis Security

Some systems feature Smart Cover (hood) Sensor and Smart Cover (hood) Lock mechanisms to inhibit unauthorized tampering of the system unit.

Smart Cover Sensor

Some systems include a plunger switch that, when the cover (hood) is removed, closes and grounds an input of the 82801 component. The battery-backed logic will record this “intrusion” event by setting a specific bit. This bit will remain set (even if the cover is replaced) until the system is powered up and the user completes the boot sequence successfully, at which time the bit will be cleared. Through Setup, the user can set this function to be used by Alert-On-LAN and or one of three levels of support for a “cover removed” condition:

Level 0—Cover removal indication is essentially disabled at this level. During POST, status bit is cleared and no other action is taken by BIOS.

Level 1—During POST the message “The computer's cover has been removed since the last system start up” is displayed and time stamp in CMOS is updated.

Level 2—During POST the “The computer's cover has been removed since the last system start up” message is displayed, time stamp in CMOS is updated, and the user is prompted for the administrator password. (A Setup password must be enabled in order to see this option).

Smart Cover Lock (Optional)

Some systems support an optional solenoid-operated locking bar that, when activated, prevents the cover (hood) from being removed. The GPIO ports 44 and 45 of the LPC47B397 I/O controller provide the lock and unlock signals to the solenoid. A locked hood may be bypassed by removing special screws that hold the locking mechanism in place. The special screws are removed with the Smart Cover Lock Failsafe Key.

4.5.2 Power Management

This system provides baseline hardware support of ACPI- and APM-compliant firmware and software. Key power-consuming components (processor, chipset, I/O controller, and fan) can be placed into a reduced power mode either automatically or by user control. The system can then be brought back up (“wake-up”) by events defined by the ACPI specification. The ACPI wake-up events supported by this system are listed as follows:

ACPI Wake-Up Event	System Wakes From
Power Button	Suspend or soft-off
RTC Alarm	Suspend or soft-off
Wake On LAN (w/NIC)	Suspend or soft-off
PME	Suspend or soft-off
Serial Port Ring	Suspend or soft-off
USB	Suspend only
Keyboard	Suspend only
Mouse	Suspend only

4.5.3 System Status

These systems provide a visual indication of system boot and ROM flash status through the keyboard LEDs and operational status using bi-colored power and hard drive activity LEDs as indicated in Tables 4-13 and 4-14 respectively.

The LED indications listed in Table 4-13 are valid only for PS/2-type keyboards. A USB keyboard will not provide LED status for the listed events, although audible (beep) indications will occur.

Table 4-13.
PS/2 Keyboard System Boot/ROM Flash Status LED Indications

Event	NUM Lock LED	CAPs Lock LED	Scroll Lock LED
System memory failure [1]	Blinking	Off	Off
Graphics controller failure [2]	Off	Blinking	Off
System failure prior to graphics cntlr. initialization [3]	Off	Off	Blinking
ROMPAQ diskette not present, faulty, or drive prob.	On	Off	Off
Password prompt	Off	On	Off
Invalid ROM detected—flash failed	Blinking [4]	Blinking [4]	Blinking [4]
Keyboard locked in network mode	Blinking [5]	Blinking [5]	Blinking [5]
Successful boot block ROM flash	On [6]	On [6]	On [6]

NOTES:
[1]Accompanied by 1 short, 2 long audio beeps
[2]Accompanied by 1 long, 2 short audio beeps
[3]Accompanied by 2 long, 1 short audio beeps
[4]All LEDs will blink in sync twice, accompanied by 1 long and three short audio beeps
[5]LEDs will blink in sequence (NUM Lock, then CAPs Lock, then Scroll Lock)
[6]Accompanied by rising audio tone.

Table 4-14 lists the audible and visible indications provided by system status conditions. .

Table 4-14.
System Operational Status LED Indications

System Status	PowerLED	Beeps [2]	Action Required
S0: System on (normal operation)	Steady green	None	none
S1: Suspend	Blinks green @ .5 Hz	None	none
S3: Suspend to RAM	Blinks green @ .5 Hz	None	none
S4: Suspend to disk	Off – clear	None	none
S5: Soft off	Off – clear	None	none
Processor thermal shutdown	Blinks red 2 times @ I Hz [1]	2 [2]	Check air flow, fans, heatsink
Processor not seated / installed	Blinks red 3 times @ I Hz [1]	3 [2]	Check processor presence/seating
Power supply overload failure	Blinks red 4 times @ I Hz [1]	4 [2]	Check voltage selector, devices, sys. bd
Memory error (pre-video)	Blinks red 5 times @ I Hz [1]	5 [2]	Check DIMMs, system board
Video error	Blinks red 6 times @ I Hz [1]	6 [2]	Check graphics card or system board
PCA failure detected by BIOS (pre-video)	Blinks red 7 times @ I Hz [1]	7 [2]	Replace system board
Invalid ROM checksum error	Blinks red 8 times @ I Hz [1]	8 [2]	Reflash BIOS ROM
Boot failure (after power on)	Blinks red 9 times @ I Hz [1]	9 [2]	Check power supply, processor, sys. bd
Bad option card	Blinks red 10 times @ I Hz [1]	10 [2]	Replace option card

[1] Repeated after 2 second pause.
[2] Beeps are produced by the on-board piezo speaker, NOT the chassis speaker.
[3] Beeps are repeated for 5 cycles, after which only blinking LED indication continues.

4.5.4 Thermal Sensing and Cooling

All systems feature a variable-speed fan mounted as part of the processor heatsink assembly. All systems also provide or support an auxiliary chassis fan. All fans are controlled through temperature sensing logic on the system board and/or in the power supply. There are some electrical differences between form factors and between some models, although the overall functionally is the same. Typical cooling conditions include the following:

1. Normal—Low fan speed.
2. Hot processor—ASIC directs Speed Control logic to increase speed of fan(s).
3. Hot power supply—Power supply increases speed of fan(s).
4. Sleep state—Fan(s) turned off. Hot processor or power supply will result in starting fan(s).

The RPM (speed) of all fans is the result of the temperature of the CPU as sensed by speed control circuitry. The fans are controlled to run at the slowest (quietest) speed that will maintain proper cooling.

Units using chassis and CPU fans must have both fans connected to their corresponding headers to ensure proper cooling of the system.

4.6 Register Map and Miscellaneous Functions

This section contains the system I/O map and information on general-purpose functions of the ICH6 and I/O controller.

4.6.1 System I/O Map

Table 4-15 lists the fixed addresses of the input/output (I/O) ports.

Table 4-15
System I/O Map

I/O Port	Function
0000..001Fh	DMA Controller 1
0020..002Dh	Interrupt Controller 1
002E, 002Fh	Index, Data Ports to LPC47B397 I/O Controller (primary)
0030..003Dh	Interrupt Controller
0040..0042h	Timer 1
004E, 004Fh	Index, Data Ports to LPC47B397 I/O Controller (secondary)
0050..0052h	Timer / Counter
0060..0067h	Microcontroller, NMI Controller (alternating addresses)
0070..0077h	RTC Controller
0080..0091h	DMA Controller
0092h	Port A, Fast A20/Reset Generator
0093..009Fh	DMA Controller
00A0..00B1h	Interrupt Controller 2
00B2h, 00B3h	APM Control/Status Ports
00B4..00BDh	Interrupt Controller
00C0..00DFh	DMA Controller 2
00F0h	Coprocessor error register
0170..0177h	IDE Controller 2 (active only if standard I/O space is enabled for primary drive)
01F0..01F7h	IDE Controller 1 (active only if standard I/O space is enabled for secondary drive)
0278..027Fh	Parallel Port (LPT2)
02E8..02EFh	Serial Port (COM4)
02F8..02FFh	Serial Port (COM2)
0370..0377h	Diskette Drive Controller Secondary Address
0376h	IDE Controller 2 (active only if standard I/O space is enabled for primary drive)
0378..037Fh	Parallel Port (LPT1)
03B0..03DFh	Graphics Controller
03BC..03BEh	Parallel Port (LPT3)
03E8..03EFh	Serial Port (COM3)
03F0..03F5h	Diskette Drive Controller Primary Addresses
03F6h	IDE Controller 1 (active only if standard I/O space is enabled for sec. drive)
03F8..03FFh	Serial Port (COM1)
04D0, 04D1h	Interrupt Controller
0678..067Fh	Parallel Port (LPT2)
0778..077Fh	Parallel Port (LPT1)
07BC..07BEh	Parallel Port (LPT3)
0CF8h	PCI Configuration Address (dword access only)
0CF9h	Reset Control Register
0CFCh	PCI Configuration Data (byte, word, or dword access)

NOTE:

Assume unmarked gaps are unused, reserved, or used by functions that employ variable I/O address mapping. Some ranges may include reserved addresses.

4.6.2 LPC47B397 I/O Controller Functions

The LPC47B397 I/O controller contains various functions such as the keyboard/mouse interfaces, diskette interface, serial interfaces, and parallel interface. While the control of these interfaces uses standard AT-type I/O addressing (as described in chapter 5) the configuration of these functions uses indexed ports unique to the LPC47B397. In these systems, hardware strapping selects I/O addresses 02Eh and 02Fh at reset as the Index/Data ports for accessing the logical devices within the LPC47B397. Table 4-16 lists the PnP standard control registers for the LPC47B397.

Table 4-16.

LPC47B397 I/O Controller Control Registers

Index	Function	Reset Value
02h	Configuration Control	00h
03h	Reserved	
07h	Logical Device (Interface) Select: 00h = Diskette Drive I/F 01h = Reserved 02h = Reserved 03h = Parallel I/F 04h = Serial I/F (UART 1/Port A) 05h = Serial I/F (UART 2/Port B) 06h = Reserved 07h = Keyboard I/F 08h = Reserved 09h = Reserved 0Ah = Runtime Registers (GPIO Config.) 0Bh = SMBus Configuration	00h
20h	Super I/O ID Register (SID)	56h
21h	Revision	–
22h	Logical Device Power Control	00h
23h	Logical Device Power Management	00h
24h	PLL / Oscillator Control	04h
25h	Reserved	
26h	Configuration Address (Low Byte)	
27h	Configuration Address (High Byte)	
28-2Fh	Reserved	

NOTE:

For a detailed description of registers refer to appropriate SMC documentation.

The configuration registers are accessed through I/O registers 2Eh (index) and 2Fh (data) after the configuration phase has been activated by writing 55h to I/O port 2Eh. The desired interface (logical device) is initiated by firmware selecting logical device number of the 47B347 using the following sequence:

1. Write 07h to I/O register 2Eh.
2. Write value of logical device to I/O register 2Fh.
3. Write 30h to I/O register 2Eh.
4. Write 01h to I/O register 2Fh (this activates the interface).

Writing AAh to 2Eh deactivates the configuration phase.

The systems covered in this guide utilize the following specialized functions built into the LPC 47B397 I/O Controller:

- Power/Hard drive LED control—The I/O controller provides color and blink control for the front panel LEDs used for indicating system events (refer to Table 4-14).
- Intruder sensing—The battery-backed D-latch logic internal to the LPC47B397 is connected to the hood sensor switch to record hood (cover) removal.
- Hood lock/unlock—Supported on SFF, ST, and CMT form factors, logic internal to the LPC47B397 controls the lock bar mechanism.
- I/O security—The parallel, serial, and diskette interfaces may be disabled individually by software and the LPC47B397's disabling register locked. If the disabling register is locked, a system reset through a cold boot is required to gain access to the disabling (Device Disable) register.
- Processor present/speed detection—One of the battery-back general-purpose inputs (GPI26) of the LPC47B397 detects if the processor has been removed. The occurrence of this event is passed to the ICH6 that will, during the next boot sequence, initiate the speed selection routine for the processor.
- Legacy/ACPI power button mode control—The LPC47B397 receives the pulse signal from the system's power button and produces the PS On signal according to the mode (legacy or ACPI) selected. Refer to chapter 7 for more information regarding power management.

5

Input/Output Interfaces

5.1 Introduction

This chapter describes the standard (i.e., system board) interfaces that provide input and output (I/O) porting of data and specifically discusses interfaces that are controlled through I/O-mapped registers. The following I/O interfaces are covered in this chapter:

5.2 PATA/SATA Interfaces

These systems provide both legacy EIDE (i.e., parallel ATA or PATA) and serial ATA (SATA) interfaces. All systems are shipped configured with SATA hard drives.

One 40-pin IDE connector is included on the system board. The controller can be configured for the following modes of operation:

- Programmed I/O (PIO) mode—CPU controls drive transactions through standard I/O mapped registers of the IDE drive.
- 8237 DMA mode—CPU offloads drive transactions using DMA protocol with transfer rates up to 16 MB/s.
- Ultra ATA/100 mode—Preferred bus mastering source-synchronous protocol providing transfer rates of 100 MB/s.

IDE Programming

The IDE interface is configured as a PCI device during POST and controlled through I/O-mapped registers at runtime. Non-DOS (non-Windows) operating systems may require using Setup (F10) for drive configuration.

IDE Configuration Registers

The IDE controller is configured as a PCI device with bus mastering capability. The PCI configuration registers for the IDE controller function (PCI device #31, function #1) are listed in Table 5-1.

Table 5-1.
EIDE PCI Configuration Registers (82801)

PCI Conf. Address	Register	Reset Value	PCI Conf. Addr.	Register	Reset Value
00-01h	Vender ID	8086h	0F..1Fh	Reserved	0's
02-03h	Device ID	[1]	20-23h	BMIDE Base Address	1
04-05h	PCI Command	0000h	2C, 2Dh	Subsystem Vender ID	0000h
06-07h	PCI Status	0280h	2E, 2Fh	Subsystem ID	0000h
08h	Revision ID	00h	30..3Fh	Reserved	0's
09h	Programming	80h	40-43h	Pri./Sec. IDE Timing	0's
0Ah	Sub-Class	01h	44h	Slave IDE Timing	00h
0Bh	Base Class Code	01h	48h	Sync. DMA Control	00h
0Dh	Master Latency Timer	00h	4A-4Bh	Sync. DMA Timing	0000h
0Eh	Header Type	00h	54h	EIDE I/O Config.Register	00h

NOTE:
[1] ICH6 = 244Bh; ICH6 = 24CBh

IDE Bus Master Control Registers

The IDE interface can perform PCI bus master operations using the registers listed in Table 5-2. These registers occupy 16 bytes of variable I/O space set by software and indicated by PCI configuration register 20h in the previous table.

Table 5-2.
IDE Bus Master Control Registers

I/O Address Offset	Size (Bytes)	Register	Default Value
00h	1	Bus Master IDE Command (Primary)	00h
02h	1	Bus Master IDE Status (Primary)	00h
04h	4	Bus Master IDE Descriptor Pointer (Pri.)	0000 0000h
08h	1	Bus Master IDE Command (Secondary)	00h
0Ah	2	Bus Master IDE Status (Secondary)	00h
0Ch	4	Bus Master IDE Descriptor Pointer (Sec.)	0000 0000h

NOTE:

Unspecified gaps are reserved, will return indeterminate data, and should not be written to.

IDE (PATA) Connector

These systems provide a standard 40-pin connector for a primary IDE device and in most factory configurations connects to a optical drive (CD or DVD). Some signals are re-defined for UATA/33 and higher modes. Device power is supplied through a separate connector.

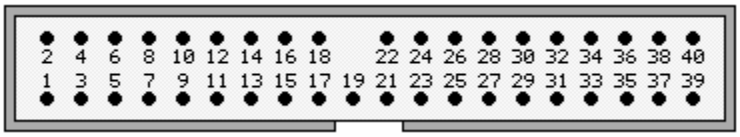


Figure 5-1. 40-Pin IDE (PATA) Connector.

Table 5-3.
40-Pin IDE (PATA) Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	RESET-	Reset	21	DRQ	DMA Request
2	GND	Ground	22	GND	Ground
3	DD7	Data Bit <7>	23	IOW-	I/O Write [1]
4	DD8	Data Bit <8>	24	GND	Ground
5	DD6	Data Bit <6>	25	IOR-	I/O Read [2]
6	DD9	Data Bit <9>	26	GND	Ground
7	DD5	Data Bit <5>	27	IORDY	I/O Channel Ready [3]
8	DD10	Data Bit <10>	28	CSEL	Cable Select
9	DD4	Data Bit <4>	29	DAK-	DMA Acknowledge
10	DD11	Data Bit <11>	30	GND	Ground
11	DD3	Data Bit <3>	31	IRQn	Interrupt Request [4]
12	DD12	Data Bit <12>	32	IO16-	16-bit I/O
13	DD2	Data Bit <2>	33	DA1	Address 1
14	DD13	Data Bit <13>	34	DSKPDIAG	Pass Diagnostics
15	DD1	Data Bit <1>	35	DA0	Address 0
16	DD14	Data Bit <14>	36	DA2	Address 2
17	DD0	Data Bit <0>	37	CS0-	Chip Select
18	DD15	Data Bit <15>	38	CS1-	Chip Select
19	GND	Ground	39	HDACTIVE-	Drive Active (front panel LED) [5]
20	--	Key	40	GND	Ground

NOTES:
[1] On UATA/33 and higher modes, re-defined as STOP.
[2] On UATA/33 and higher mode reads, re-defined as DMARDY-.
On UATA/33 and higher mode writes, re-defined as STROBE.
[3] On UATA/33 and higher mode reads, re-defined as STROBE-.
On UATA/33 and higher mode writes, re-defined as DMARDY-.
[4] Primary connector wired to IRQ14, secondary connector wired to IRQ15.
[5] Pin 39 is used for spindle sync and drive activity (becomes SPSYNC/DACT-)
when synchronous drives are connected.

SATA Interfaces

These systems provide one, two, or four serial ATA (SATA) interfaces that can provide certain advantages over legacy EIDE (PATA) interface including:

- Higher transfer rates: up to 1.5 Gb/s (150 MB/s)
- Reduced wiring (smaller cable assemblies)

The SATA interface duplicates most of the functionality of the EIDE interface through a register interface that is equivalent to that of the legacy IDE host adapter.

SATA Programming

The SATA interface is configured as a PCI device during POST and controlled through I/O-mapped registers at runtime. Non-DOS (non-Windows) operating systems may require using Setup (F10) for drive configuration.

SATA Configuration Registers

The SATA controller is configured as a PCI device with bus mastering capability. The PCI configuration registers for the SATA controller function (PCI device #31, function #2) are listed in Table 5-4.

Table 5-4.
SATA PCI Configuration Registers (82801, Device 31/Function 2)

PCI Conf. Addr.	Register	Reset Value	PCI Conf. Addr.	Register	Reset Value
00-01h	Vender ID	8086h	0F..1Fh	Reserved	0's
02-03h	Device ID	24D1h	10-17h	Pri. Cmd, Cntrl. Addrs.	1 (both)
04-05h	PCI Command	0000h	18-1Fh	Sec. Cmd, Cntrl. Addrs.	1 (both)
06-07h	PCI Status	02B0h	20-23h	BMstr Base Address	1
08h	Revision ID	00h	2C, 2Dh	Subsystem Vender ID	0000h
09h	Programming	8Ah	2E, 2Fh	Subsystem ID	0000h
0Ah	Sub-Class	01h	34h	Capabilities pointer	80h
0Bh	Base Class Code	01h	3Ch	Interrupt Line	00h
0Dh	Master Latency Timer	00h	3Dh	Interrupt Pin	01h
0Eh	Header Type	00h	40-57h	Timing, Control	All 0's

SATA Bus Master Control Registers

The SATA interface can perform PCI bus master operations using the registers listed in Table 5-5. These registers occupy 16 bytes of variable I/O space set by software and indicated by PCI configuration register 20h in the previous table. As indicated, these registers are virtually a copy of those used by EIDE operations discussed in the EIDE section.

Table 5-5.
IDE Bus Master Control Registers

I/O Addr. Offset	Size (Bytes)	Register	Default Value
00h	1	Bus Master IDE Command (Primary)	00h
02h	1	Bus Master IDE Status (Primary)	00h
04h	4	Bus Master IDE Descriptor Pointer (Primary)	0000 0000h
08h	1	Bus Master IDE Command (Secondary)	00h
0Ah	2	Bus Master IDE Status (Secondary)	00h
0Ch	4	Bus Master IDE Descriptor Pointer (Secondary	0000 0000h

SATA Connector

The 7-pin SATA connector is shown in the figure below.

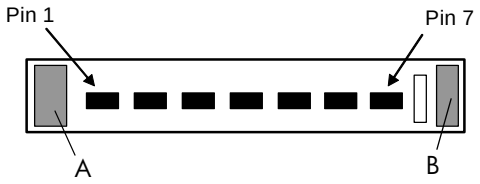


Figure 5-2. 7-Pin SATA Connector (on system board).

Table 5-6.
7-Pin SATA Connector Pinout

Pin	Description	Pin	Description
1	Ground	6	RX positive
2	TX positive	7	Ground
3	TX negative	A	Holding clip
4	Ground	B	Holding clip
5	RX negative	--	--

5.3 Diskette Drive Interface

The diskette drive interface in these systems support one diskette drive connected to a standard 34-pin diskette drive connector. Selected models come standard with a 3.5-inch 1.44-MB diskette drive installed as drive A.

The diskette drive interface function is integrated into the LPC47B397 super I/O component. The internal logic of the I/O controller is software-compatible with standard 82077-type logic. The diskette drive controller has three operational phases in the following order:

- Command phase—The controller receives the command from the system.
- Execution phase—The controller carries out the command.
- Results phase—Status and results data is read back from the controller to the system.

The Command phase consists of several bytes written in series from the CPU to the data register (3F5h/375h). The first byte identifies the command and the remaining bytes define the parameters of the command. The Main Status register (3F4h/374h) provides data flow control for the diskette drive controller and must be polled between each byte transfer during the Command phase.

The Execution phase starts as soon as the last byte of the Command phase is received. An Execution phase may involve the transfer of data to and from the diskette drive, a mechnical control function of the drive, or an operation that remains internal to the diskette drive controller.

Data transfers (writes or reads) with the diskette drive controller are by DMA, using the DRQ2 and DACK2- signals for control.

The Results phase consists of the CPU reading a series of status bytes (from the data register (3F5h/375h)) that indicate the results of the command. Note that some commands do not have a Result phase, in which case the Execution phase can be followed by a Command phase.

During periods of inactivity, the diskette drive controller is in a non-operation mode known as the Idle phase.

5.3.1 Diskette Drive Programming

Programming the diskette drive interface consists of configuration, which occurs typically during POST, and control, which occurs at runtime.

Diskette Drive Interface Configuration

The diskette drive controller must be configured for a specific address and also must be enabled before it can be used. Address selection and enabling of the diskette drive interface are affected by firmware through the PnP configuration registers of the 47B397 I/O controller during POST.

The configuration registers are accessed through I/O registers 2Eh (index) and 2Fh (data) after the configuration phase has been activated by writing 55h to I/O port 2Eh. The diskette drive I/F is initiated by firmware selecting logical device 0 of the 47B397 using the following sequence:

1. Write 07h to I/O register 2Eh.
2. Write 00h to I/O register 2Fh (this selects the diskette drive I/F).
3. Write 30h to I/O register 2Eh.
4. Write 01h to I/O register 2Fh (this activates the interface).

Writing AAh to 2Eh deactivates the configuration phase. The diskette drive I/F configuration registers are listed in the following table:

Table 5-7.
Diskette Drive Interface Configuration Registers

Index Address	Function	R/W	Reset Value
30h	Activate	R/W	01h
60-61h	Base Address	R/W	03F0h
70h	Interrupt Select	R/W	06h
74h	DMA Channel Select	R/W	02h
F0h	DD Mode	R/W	02h
F1h	DD Option	R/W	00h
F2h	DD Type	R/W	FFh
F4h	DD 0	R/W	00h
F5h	DD 1	R/W	00h

For detailed configuration register information refer to the SMSC data sheet for the LPC47B397 I/O component.

Diskette Drive Interface Control

The BIOS function INT 13 provides basic control of the diskette drive interface. The diskette drive interface can be controlled by software through the LPC47B397's I/O-mapped registers listed in Table 5-8. The diskette drive controller of the LPC47B397 operates in the PC/AT mode in these systems.

Table 5-8.
Diskette Drive Interface Control Registers

Primary Address	Second. Address	Register	R/W
3F0h	370h	Status Register A: <7> Interrupt pending <6> Reserved (always 1) <5> STEP pin status (active high) <4> TRK 0 status (active high) <3> HDSEL status (0 = side 0, 1 = side 1) <2> INDEX status (active high) <1> WR PRTK status (0 = disk is write protected) <0> Direction (0 = outward, 1 = inward)	R
3F1h	371h	Status Register B: <7,6> Reserved (always 1's) <5> DOR bit 0 status <4> Write data toggle <3> Read data toggle <2> WGATE status (active high) <1,0> MTR 2, 1 ON- status (active high)	R
3F2h	372h	Digital Output Register (DOR): <7,6> Reserved <5,4> Motor 1, 0 enable (active high) <3> DMA enable (active high) <2> Reset (active low) <1,0> Drive select (00 = Drive 1, 01 = Drive 2, 10 = Reserved, 11 = Tape drive)	R/W
3F3h	373h	Tape Drive Register (available for compatibility)	R/W

Table 5-8. *(Continued)*
Diskette Drive Interface Control Registers

Primary Address	Second. Address	Register	R/W
3F4h	374h	Main Status Register (MSR): <7> Request for master (host can transfer data) (active high) <6> Transfer direction (0 – write, 1 = read) <5> non-DMA execution (active high) <4> Command busy (active high) <3,2> Reserved <1,0> Drive 1, 2 busy (active high)	R
		Data Rate Select Register (DRSR): <7> Software reset (active high) <6> Low power mode enable (active high) <5> Reserved (0) <4..2> Precompensation select (default = 000) <1,0> Data rate select (00 = 500 Kb/s, 01 = 300 Kb/s, 10 = 250 Kb/s, 11 = 2/1 Mb/s)	W
3F5h	375h	Data Register: <7..0> Data	R/W
3F6h	376h	Reserved	–
3F7h	377h	Digital Input Register (DIR): <7> DSK CHG status (records opposite value of pin) <6..0> Reserved (0's)	R
		Configuration Control Register (CCR): <7..2> Reserved <1,0> Data rate select (00 = 500 Kb/s, 01 = 300 Kb/s, 10 = 250 Kb/s, 11 = 2/1 Mb/s)	W

NOTE: The most recently written data rate value to either DRSR or CCR will be in effect.

5.3.2 Diskette Drive Connector

This system uses a standard 34-pin connector (refer to Figure 5-3 and Table 5-9 for the pinout) for diskette drives. Drive power is supplied through a separate connector.

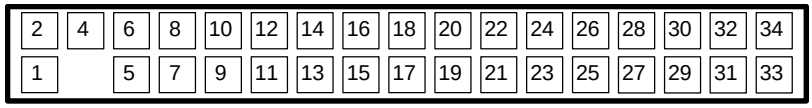


Figure 5-3. 34-Pin Diskette Drive Connector.

Table 5-9.
34-Pin Diskette Drive Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	18	DIR-	Drive head direction control
2	LOW DEN-	Low density select	19	GND	Ground
3	---	(KEY)	20	STEP-	Drive head track step cntrl.
4	MEDIA ID-	Media identification	21	GND	Ground
5	GND	Ground	22	WR DATA-	Write data
6	DRV 4 SEL-	Drive 4 select	23	GND	Ground
7	GND	Ground	24	WR ENABLE-	Enable for WR DATA-
8	INDEX-	Media index is detected	25	GND	Ground
9	GND	Ground	26	TRK 00-	Heads at track 00 indicator
10	MTR 1 ON-	Activates drive motor	27	GND	Ground
11	GND	Ground	28	WR PRTK-	Media write protect status
12	DRV 2 SEL-	Drive 2 select	29	GND	Ground
13	GND	Ground	30	RD DATA-	Data and clock read off disk
14	DRV 1 SEL-	Drive 1 select	31	GND	Ground
15	GND	Ground	32	SIDE SEL-	Head select (side 0 or 1)
16	MTR 2 ON-	Activates drive motor	33	GND	Ground
17	GND	Ground	34	DSK CHG-	Drive door opened indicator

5.4 Serial Interface

Systems covered in this guide may include one RS-232-C type serial interface to transmit and receive asynchronous serial data with external devices. Some systems may allow the installation of a second serial interface through an adapter that consists of a PCI bracket and a cable that attaches to header P52 on the system board. The serial interface function is provided by the LPC47B397 I/O controller component that includes two NS16C550-compatible UARTs.

The UART supports the standard baud rates up through 115200, and also special high speed rates of 239400 and 460800 baud. The baud rate of the UART is typically set to match the capability of the connected device. While most baud rates may be set at runtime, baud rates 230400 and 460800 must be set during the configuration phase.

5.4.1 Serial Connector

The serial interface uses a DB-9 connector as shown in the following figure with the pinout listed in Table 5-10.

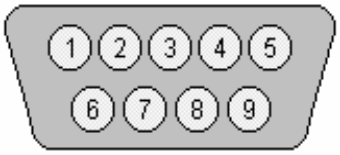


Figure 5-4. Serial Interface Connector (Male DB-9 as viewed from rear of chassis)

Table 5-10.
DB-9 Serial Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	CD	Carrier Detect	6	DSR	Data Set Ready
2	RX Data	Receive Data	7	RTS	Request To Send
3	TX Data	Transmit Data	8	CTS	Clear To Send
4	DTR	Data Terminal Ready	9	RI	Ring Indicator
5	GND	Ground	--	--	--

The standard RS-232-C limitation of 50 feet (or less) of cable between the DTE (computer) and DCE (modem) should be followed to minimize transmission errors. Higher baud rates may require shorter cables.

5.4.2 Serial Interface Programming

Programming the serial interfaces consists of configuration, which occurs during POST, and control, which occurs during runtime.

Serial Interface Configuration

The serial interface must be configured for a specific address range (COM1, COM2, etc.) and also must be activated before it can be used. Address selection and activation of the serial interface are affected through the PnP configuration registers of the LPC47B397 I/O controller.

The serial interface configuration registers are listed in the following table:

Table 5-11.
Serial Interface Configuration Registers

Index Address	Function	R/W
30h	Activate	R/W
60h	Base Address MSB	R/W
61h	Base Address LSB	R/W
70h	Interrupt Select	R/W
F0h	Mode Register	R/W

Serial Interface Control

The BIOS function INT 14 provides basic control of the serial interface. The serial interface can be directly controlled by software through the I/O-mapped registers listed in Table 5-12.

Table 5-12.
Serial Interface Control Registers

COM1 Addr.	COM2 Addr.	Register	R/W
3F8h	2F8h	Receive Data Buffer	R
		Transmit Data Buffer	W
		Baud Rate Divisor Register 0 (when bit 7 of Line Control Reg. Is set)	W
3F9h	2F9h	Baud Rate Divisor Register 1 (when bit 7 of Line Control Reg. Is set)	W
		Interrupt Enable Register	R/W
3FAh	2FAh	Interrupt ID Register	R
		FIFO Control Register	W
3FBh	2FBh	Line Control Register	R/W
3FCh	2FCh	Modem Control Register	R/W
3FDh	2FDh	Line Status Register	R
3FEh	2FEh	Modem Status	R

5.5 Parallel Interface

Systems covered in this guide may include a parallel interface for connection to a peripheral device with a compatible interface, the most common being a printer. The parallel interface function is integrated into the LPC47B397 I/O controller component and provides bi-directional 8-bit parallel data transfers with a peripheral device. The parallel interface supports three main modes of operation:

- Standard Parallel Port (SPP) mode
- Enhanced Parallel Port (EPP) mode
- Extended Capabilities Port (ECP) mode

These three modes (and their submodes) provide complete support as specified for an IEEE 1284 parallel port.

5.5.1 Standard Parallel Port Mode

The Standard Parallel Port (SPP) mode uses software-based protocol and includes two sub-modes of operation, compatible and extended, both of which can provide data transfers up to 150 KB/s. In the compatible mode, CPU write data is simply presented on the eight data lines. A CPU read of the parallel port yields the last data byte that was written.

The following steps define the standard procedure for communicating with a printing device:

1. The system checks the Printer Status register. If the Busy, Paper Out, or Printer Fault signals are indicated as being active, the system either waits for a status change or generates an error message.
2. The system sends a byte of data to the Printer Data register, then pulses the printer STROBE signal (through the Printer Control register) for at least 500 ns.
3. The system then monitors the Printer Status register for acknowledgment of the data byte before sending the next byte.

In extended mode, a direction control bit (CTR 37Ah, bit <5>) controls the latching of output data while allowing a CPU read to fetch data present on the data lines, thereby providing bi-directional parallel transfers to occur.

The SPP mode uses three registers for operation: the Data register (DTR), the Status register (STR) and the Control register (CTR). Address decoding in SPP mode includes address lines A0 and A1.

5.5.2 Enhanced Parallel Port Mode

In Enhanced Parallel Port (EPP) mode, increased data transfers are possible (up to 2 MB/s) due to a hardware protocol that provides automatic address and strobe generation. EPP revisions 1.7 and 1.9 are both supported. For the parallel interface to be initialized for EPP mode, a negotiation phase is entered to detect whether or not the connected peripheral is compatible with EPP mode. If compatible, then EPP mode can be used. In EPP mode, system timing is closely coupled to EPP timing. A watchdog timer is used to prevent system lockup.

Five additional registers are available in EPP mode to handle 16- and 32-bit CPU accesses with the parallel interface. Address decoding includes address lines A0, A1, and A2.

5.5.3 Extended Capabilities Port Mode

The Extended Capabilities Port (ECP) mode, like EPP, also uses a hardware protocol-based design that supports transfers up to 2 MB/s. Automatic generation of addresses and strobes as well as Run Length Encoding (RLE) decompression is supported by ECP mode. The ECP mode includes a bi-directional FIFO buffer that can be accessed by the CPU using DMA or programmed I/O. For the parallel interface to be initialized for ECP mode, a negotiation phase is entered to detect whether or not the connected peripheral is compatible with ECP mode. If compatible, then ECP mode can be used.

Ten control registers are available in ECP mode to handle transfer operations. In accessing the control registers, the base address is determined by address lines A2-A9, with lines A0, A1, and A10 defining the offset address of the control register. Registers used for FIFO operations are accessed at their base address + 400h (i.e., if configured for LPT1, then 378h + 400h = 778h).

The ECP mode includes several sub-modes as determined by the Extended Control register. Two submodes of ECP allow the parallel port to be controlled by software. In these modes, the FIFO is cleared and not used, and DMA and RLE are inhibited.

5.5.4 Parallel Interface Programming

Programming the parallel interface consists of configuration, which typically occurs during POST, and control, which occurs during runtime.

Parallel Interface Configuration

The parallel interface must be configured for a specific address range (LPT1, LPT2, etc.) and also must be enabled before it can be used. When configured for EPP or ECP mode, additional considerations must be taken into account. Address selection, enabling, and EPP/ECP mode parameters of the parallel interface are affected through the PnP configuration registers of the LPC47B397 I/O controller. Address selection and enabling are automatically done by the BIOS during POST but can also be accomplished with the Setup utility and other software.

The parallel interface configuration registers are listed in the following table:

Table 5-13.
Parallel Interface Configuration Registers

Index Address	Function	R/W	Reset Value
30h	Activate	R/W	00h
60h	Base Address MSB	R/W	00h
61h	Base Address LSB	R/W	00h
70h	Interrupt Select	R/W	00h
74h	DMA Channel Select	R/W	04h
F0h	Mode Register	R/W	00h
F1h	Mode Register 2	R/W	00h

Parallel Interface Control

The BIOS function INT 17 provides simplified control of the parallel interface. Basic functions such as initialization, character printing, and printer status are provide by subfunctions of INT 17. The parallel interface is controllable by software through a set of I/O mapped registers. The number and type of registers available depends on the mode used (SPP, EPP, or ECP). Table 5-14 lists the parallel registers and associated functions based on mode.

Table 5-14.
Parallel Interface Control Registers

I/O Address	Register	SPP Mode Ports	EPP Mode Ports	ECP Mode Ports
Base	Data	LPT1,2,3	LPT1,2	LPT1,2,3
Base + 1h	Printer Status	LPT1,2,3	LPT1,2	LPT1,2,3
Base + 2h	Control	LPT1,2,3	LPT1,2	LPT1,2,3
Base + 3h	Address	--	LPT1,2	--
Base + 4h	Data Port 0	--	LPT1,2	--
Base + 5h	Data Port 1	--	LPT1,2	--
Base + 6h	Data Port 2	--	LPT1,2	--
Base + 7h	Data Port 3	--	LPT1,2	--
Base + 400h	Parallel Data FIFO	--	--	LPT1,2,3
Base + 400h	ECP Data FIFO	--	--	LPT1,2,3
Base + 400h	Test FIFO	--	--	LPT1,2,3
Base + 400h	Configuration Register A	--	--	LPT1,2,3
Base + 401h	Configuration Register B	--	--	LPT1,2,3
Base + 402h	Extended Control Register	--	--	LPT1,2,3

Base Address:
LPT1 = 378h
LPT2 = 278h
LPT3 = 3BCh

5.5.5 Parallel Interface Connector

Figure 5-5 and Table 5-15 show the connector and pinout of the parallel interface connector. Note that some signals are redefined depending on the port's operational mode.

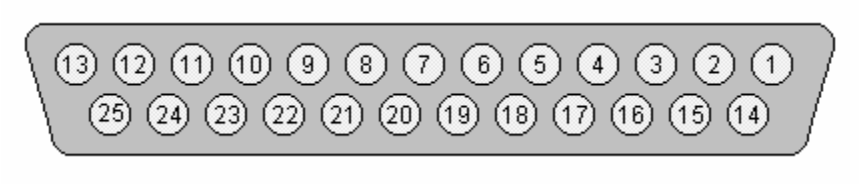


Figure 5-5. Parallel Interface Connector (Female DB-25 as viewed from rear of chassis)

Table 5-15.
DB-25 Parallel Connector Pinout

Pin	Signal	Function	Pin	Signal	Function
1	STB-	Strobe / Write [1]	14	LF-	Line Feed [2]
2	D0	Data 0	15	ERR-	Error [3]
3	D1	Data 1	16	INIT-	Initialize Paper [4]
4	D2	Data 2	17	SLCTIN-	Select In / Address. Strobe [1]
5	D3	Data 3	18	GND	Ground
6	D4	Data 4	19	GND	Ground
7	D5	Data 5	20	GND	Ground
8	D6	Data 6	21	GND	Ground
9	D7	Data 7	22	GND	Ground
10	ACK-	Acknowledge / Interrupt [1]	23	GND	Ground
11	BSY	Busy / Wait [1]	24	GND	Ground
12	PE	Paper End / User defined [1]	25	GND	Ground
13	SLCT	Select / User defined [1]	–	--	--

NOTES:

[1] Standard and ECP mode function / EPP mode function

[2] EPP mode function: Data Strobe
ECP modes: Auto Feed or Host Acknowledge

[3] EPP mode: user defined
ECP modes:Fault or Peripheral Req.

[4] EPP mode: Reset
ECP modes: Initialize or Reverse Req.

5.6 Keyboard/Pointing Device Interface

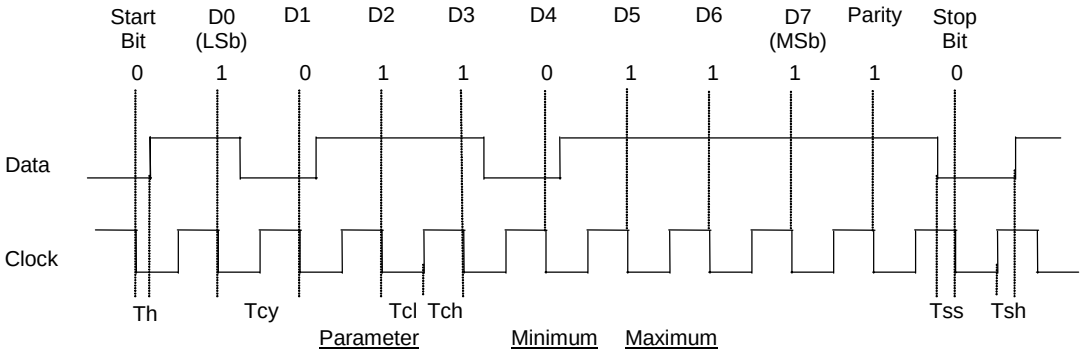
The keyboard/pointing device interface function is provided by the LPC47B397 I/O controller component, which integrates 8042-compatible keyboard controller logic (hereafter referred to as simply the “8042”) to communicate with the keyboard and pointing device using bi-directional serial data transfers. The 8042 handles scan code translation and password lock protection for the keyboard as well as communications with the pointing device. This section describes the interface itself. The keyboard is discussed in the Appendix C.

5.6.1 Keyboard Interface Operation

The data/clock link between the 8042 and the keyboard is uni-directional for Keyboard Mode 1 and bi-directional for Keyboard Modes 2 and 3. (These modes are discussed in detail in Appendix C). This section describes Mode 2 (the default) mode of operation.

Communication between the keyboard and the 8042 consists of commands (originated by either the keyboard or the 8042) and scan codes from the keyboard. A command can request an action or indicate status. The keyboard interface uses IRQ1 to get the attention of the CPU.

The 8042 can send a command to the keyboard at any time. When the 8042 wants to send a command, the 8042 clamps the clock signal from the keyboard for a minimum of 60 us. If the keyboard is transmitting data at that time, the transmission is allowed to finish. When the 8042 is ready to transmit to the keyboard, the 8042 pulls the data line low, causing the keyboard to respond by pulling the clock line low as well, allowing the start bit to be clocked out of the 8042. The data is then transferred serially, LSb first, to the keyboard (Figure 5-6). An odd parity bit is sent following the eighth data bit. After the parity bit is received, the keyboard pulls the data line low and clocks this condition to the 8042. When the keyboard receives the stop bit, the clock line is pulled low to inhibit the keyboard and allow it to process the data.



Parameter	Minimum	Maximum
Tcy (Cycle Time)	0 us	80 us
Tcl (Clock Low)	25 us	35 us
Tch (Clock High)	25 us	45 us
Th (Data Hold)	0 us	25 us
Tss (Stop Bit Setup)	8 us	20 us
Tsh (Stop Bit Hold)	15 us	25 us

Figure 5-6. 8042-To-Keyboard Transmission of Code EDh, Timing Diagram

Control of the data and clock signals is shared by the 8042and the keyboard depending on the originator of the transferred data. Note that the clock signal is always generated by the keyboard.

After the keyboard receives a command from the 8042, the keyboard returns an ACK code. If a parity error or timeout occurs, a Resend command is sent to the 8042.

Table 5-16 lists and describes commands that can be issued by the 8042 to the keyboard.

Table 5-16.
8042-To-Keyboard Commands

Command	Value	Description
Set/Reset Status Indicators	EDh	Enables LED indicators. Value EDh is followed by an option byte that specifies the indicator as follows: Bits <7..3> not used Bit <2>, Caps Lock (0 = off, 1 = on) Bit <1>, NUM Lock (0 = off, 1 = on) Bit <0>, Scroll Lock (0 = off, 1 = on)
Echo	EEh	Keyboard returns EEh when previously enabled.
Invalid Command	EFh/F1h	These commands are not acknowledged.
Select Alternate Scan Codes	F0h	Instructs the keyboard to select another set of scan codes and sends an option byte after ACK is received: 01h = Mode 1 02h = Mode 2 03h = Mode 3
Read ID	F2h	Instructs the keyboard to stop scanning and return two keyboard ID bytes.
Set Typematic Rate/Display	F3h	Instructs the keyboard to change typematic rate and delay to specified values: Bit <7>, Reserved—0 Bits <6,5>, Delay Time 00 = 250 ms 01 = 500 ms 10 = 750 ms 11 = 1000 ms Bits <4..0>, Transmission Rate: 00000 = 30.0 ms 00001 = 26.6 ms 00010 = 24.0 ms 00011 = 21.8 ms : 11111 = 2.0 ms
Enable	F4h	Instructs keyboard to clear output buffer and last typematic key and begin key scanning.
Default Disable	F5h	Resets keyboard to power-on default state and halts scanning pending next 8042 command.
Set Default	F6h	Resets keyboard to power-on default state and enable scanning.
Set Keys—Typematic	F7h	Clears keyboard buffer and sets default scan code set. [1]

Table 5-16. *(Continued)*
8042-To-Keyboard Commands

Command	Value	Description
Set Keys—Make/Brake	F8h	Clears keyboard buffer and sets default scan code set. [1]
Set Keys—Make	F9h	Clears keyboard buffer and sets default scan code set. [1]
Set Keys—Typematic/Make/Brake	FAh	Clears keyboard buffer and sets default scan code set. [1]
Set Type Key—Typematic	FBh	Clears keyboard buffer and prepares to receive key ID. [1]
Set Type Key—Make/Brake	FCh	Clears keyboard buffer and prepares to receive key ID. [1]
Set Type Key—Make	FDh	Clears keyboard buffer and prepares to receive key ID. [1]
Resend	FEh	8042 detected error in keyboard transmission.
Reset	FFh	Resets program, runs keyboard BAT, defaults to Mode 2.

Note: [1] Used in Mode 3 only.

5.6.2 Pointing Device Interface Operating

The pointing device (typically a mouse) connects to a 6-pin DIN-type connector that is identical to the keyboard connector both physically and electrically. The operation of the interface (clock and data signal control) is the same as for the keyboard. The pointing device interface uses the IRQ12 interrupt.

5.6.3 Keyboard/Pointing Device Interface Programming

Programming the keyboard interface consists of configuration, which occurs during POST, and control, which occurs during runtime.

8042 Configuration

The keyboard/pointing device interface must be enabled and configured for a particular speed before it can be used. Enabling and speed parameters of the 8042 logic are affected through the PnP configuration registers of the LPC47B397 I/O controller. Enabling and speed control are automatically set by the BIOS during POST but can also be accomplished with the Setup utility and other software.

The keyboard interface configuration registers are listed in the following table:

Table 5-17.
Keyboard Interface Configuration Registers

Index Address	Function	R/W
30h	Activate	R/W
70h	Primary Interrupt Select	R/W
72h	Secondary Interrupt Select	R/W
F0h	Reset and A20 Select	R/W

8042 Control

The BIOS function INT 16 is typically used for controlling interaction with the keyboard. Sub-functions of INT 16 conduct the basic routines of handling keyboard data (i.e., translating the keyboard's scan codes into ASCII codes). The keyboard/pointing device interface is accessed by the CPU through I/O mapped ports 60h and 64h, which provide the following functions:

- Output buffer reads
- Input buffer writes
- Status reads
- Command writes

Ports 60h and 64h can be accessed using the IN instruction for a read and the OUT instruction for a write. Prior to reading data from port 60h, the “Output Buffer Full” status bit (64h, bit <0>) should be checked to ensure data is available. Likewise, before writing a command or data, the “Input Buffer Empty” status bit (64h, bit <1>) should also be checked to ensure space is available.

I/O Port 60h

I/O port 60h is used for accessing the input and output buffers. This register is used to send and receive data from the keyboard and the pointing device. This register is also used to send the second byte of multi-byte commands to the 8042 and to receive responses from the 8042 for commands that require a response.

A read of 60h by the CPU yields the byte held in the output buffer. The output buffer holds data that has been received from the keyboard and is to be transferred to the system.

A CPU write to 60h places a data byte in the input byte buffer and sets the CMD/ DATA bit of the Status register to DATA. The input buffer is used for transferring data from the system to the keyboard. All data written to this port by the CPU will be transferred to the keyboard except bytes that follow a multibyte command that was written to 64h

I/O Port 64h

I/O port 64h is used for reading the status register and for writing commands. A read of 64h by the CPU will yield the status byte defined as follows:

Bit	Function
7..4	General Purpose Flags.
3	CMD/DATA Flag (reflects the state of A2 during a CPU write). 0 = Data 1 = Command
2	General Purpose Flag.
1	Input Buffer Full. Set (to 1) upon a CPU write. Cleared by IN A, DBB instruction.
0	Output Buffer Full (if set). Cleared by a CPU read of the buffer.

A CPU write to I/O port 64h places a command value into the input buffer and sets the CMD/DATA bit of the status register (bit <3>) to CMD.

Table 5-18 lists the commands that can be sent tothe 8042 by the CPU. The 8042 uses IRQ1 for gaining the attention of the CPU.

Table 5-18.
CPU Commands to the 8042

Value	Command Description
20h	Put current command byte in port 60h.
60h	Load new command byte.
A4h	Test password installed. Tests whether or not a password is installed in the 8042: If FAh is returned, password is installed. If F1h is returned, no password is installed.
A5h	Load password. This multi-byte operation places a password in the 8042 using the following manner: 1. Write A5h to port 64h. 2. Write each character of the password in 9-bit scan code (translated) format to port 60h. 3. Write 00h to port 60h.
A6h	Enable security. This command places the 8042 in password lock mode following the A5h command. The correct password must then be entered before further communication with the 8042 is allowed.
A7h	Disable pointing device. This command sets bit <5> of the 8042 command byte, pulling the clock line of the pointing device interface low.
A8h	Enable pointing device. This command clears bit <5> of the 8042 command byte, activating the clock line of the pointing device interface.

Table 5-18. *(Continued)*
CPU Commands to the 8042

Value	Command Description
A9h	Test the clock and data lines of the pointing device interface and place test results in the output buffer. 00h = No error detected 01h = Clock line stuck low 02h = Clock line stuck high 03h = Data line stuck low 04h = Data line stuck high
AAh	Initialization. This command causes the 8042 to inhibit the keyboard and pointing device and places 55h into the output buffer.
ABh	Test the clock and data lines of the keyboard interface and place test results in the output buffer. 00h = No error detected 01h = Clock line stuck low 02h = Clock line stuck high 03h = Data line stuck low 04h = Data line stuck high
ADh	Disable keyboard command (sets bit <4> of the 8042 command byte).
AEh	Enable keyboard command (clears bit <4> of the 8042 command byte).
C0h	Read input port of the 8042. This command directs the 8042 to transfer the contents of the input port to the output buffer so that they can be read at port 60h.
C2h	Poll Input Port High. This command directs the 8042 to place bits <7..4> of the input port into the upper half of the status byte on a continous basis until another command is received.
C3h	Poll Input Port Low. This command directs the 8042 to place bits <3..0> of the input port into the lower half of the status byte on a continous basis until another command is received.
D0h	Read output port. This command directs the 8042 to transfer the contents of the output port to the output buffer so that they can be read at port 60h.
D1h	Write output port. This command directs the 8042 to place the next byte written to port 60h into the output port (only bit <1> can be changed).
D2h	Echo keyboard data. Directs the 8042 to send back to the CPU the next byte written to port 60h as if it originated from the keyboard. No 11-to-9 bit translation takes place but an interrupt (IRQ1) is generated if enabled.
D3h	Echo pointing device data. Directs the 8042 to send back to the CPU the next byte written to port 60h as if it originated from the pointing device. An interrupt (IRQ12) is generated if enabled.
D4h	Write to pointing device. Directs the 8042 to send the next byte written to 60h to the pointing device.
E0h	Read test inputs. Directs the 8042 to transfer the test bits 1 and 0 into bits <1,0> of the output buffer.
F0h-FFh	Pulse output port. Controls the pulsing of bits <3..0> of the output port (0 = pulse, 1 = don't pulse). Note that pulsing bit <0> will reset the system.

5.6.4 Keyboard/Pointing Device Interface Connector

The legacy-light model provides separate PS/2 connectors for the keyboard and pointing device. Both connectors are identical both physically and electrically. Figure 5-7 and Table 5-19 show the connector and pinout of the keyboard/pointing device interface connectors.

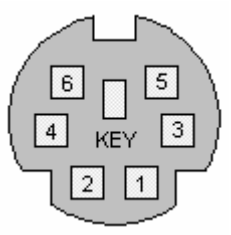


Figure 5-7. PS/2 Keyboard or Pointing Device Interface Connector (as viewed from rear of chassis)

Table 5-19.
Keyboard/Pointing Device Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	DATA	Data	4	+ 5 VDC	Power
2	NC	Not Connected	5	CLK	Clock
3	GND	Ground	6	NC	Not Connected

5.7 Universal Serial Bus Interface

The Universal Serial Bus (USB) interface provides asynchronous/isochronous data transfers with compatible peripherals such as keyboards, printers, or modems. This high-speed interface supports hot-plugging of compatible devices, making possible system configuration changes without powering down or even rebooting systems.

As shown in Figure 5-8, the USB interface is provided by the 82801 component. All systems provide as total of eight USB ports, two USB ports accessible at the front of the unit and six USB ports on the rear panel. The USB ports are dynamically configured to either a USB 1.1 controller or the USB 2.0 controller depending on the capability of the peripheral device. The 1.1 controllers provide a maximum transfer rate of 12 Mb/s while the 2.0 controller provides a maximum transfer rate of 480 Mb/s.

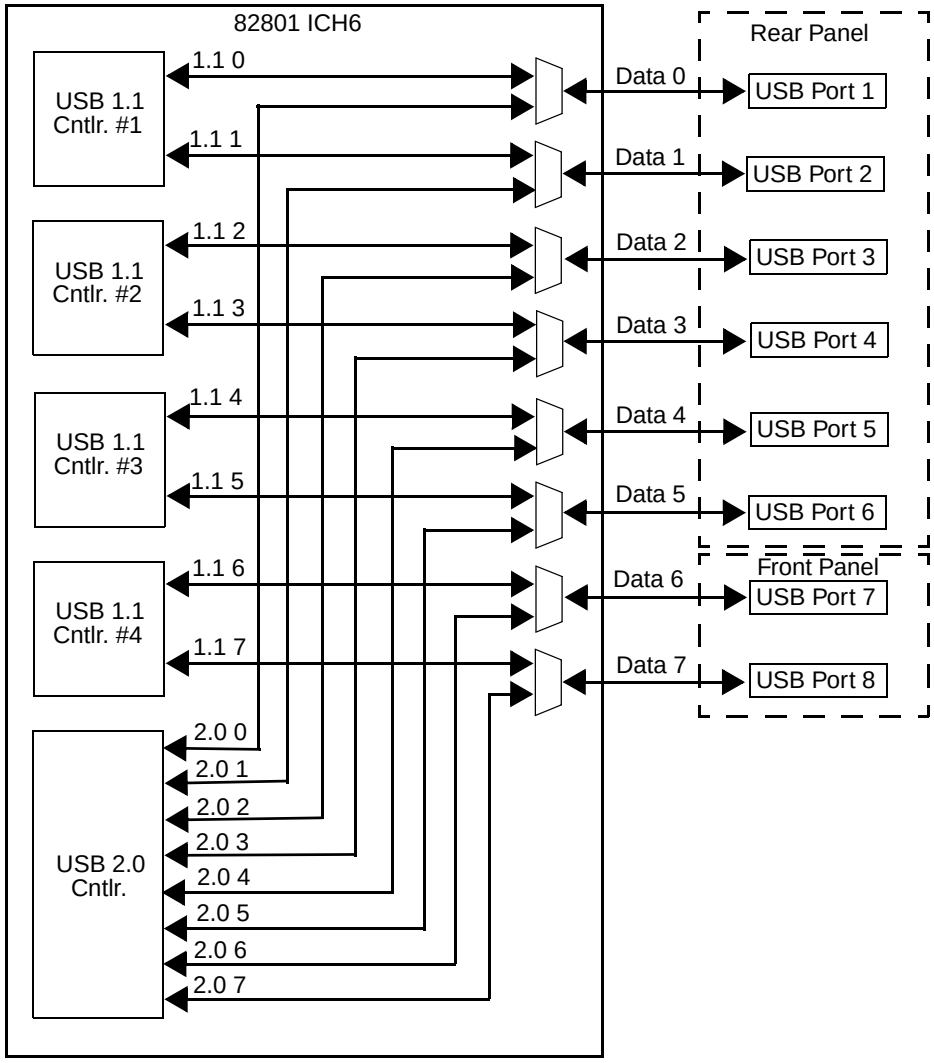


Figure 5-8. USB I/F, Block Diagram

5.7.1 USB Data Formats

The USB I/F uses non-return-to-zero inverted (NRZI) encoding for data transmissions, in which a 1 is represented by no change (between bit times) in signal level and a 0 is represented by a change in signal level. Bit stuffing is employed prior to NRZ1 encoding so that in the event a string of 1's is transmitted (normally resulting in a steady signal level) a 0 is inserted after every six consecutive 1's to ensure adequate signal transitions in the data stream. The USB transmissions consist of packets using one of four types of formats (Figure 5-9) that include two or more of seven field types.

- Sync Field—8-bit field that starts every packet and is used by the receiver to align the incoming signal with the local clock.
- Packet Identifier (PID) Field—8-bit field sent with every packet to identify the attributes (in. out, start-of-frame (SOF), setup, data, acknowledge, stall, preamble) and the degree of error correction to be applied.
- Address Field—7-bit field that provides source information required in token packets.
- Endpoint Field—4-bit field that provides destination information required in token packets.
- Frame Field—11-bit field sent in Start-of-Frame (SOF) packets that are incremented by the host and sent only at the start of each frame.
- Data Field—0-1023-byte field of data.
- Cyclic Redundancy Check (CRC) Field—5- or 16-bit field used to check transmission integrity.

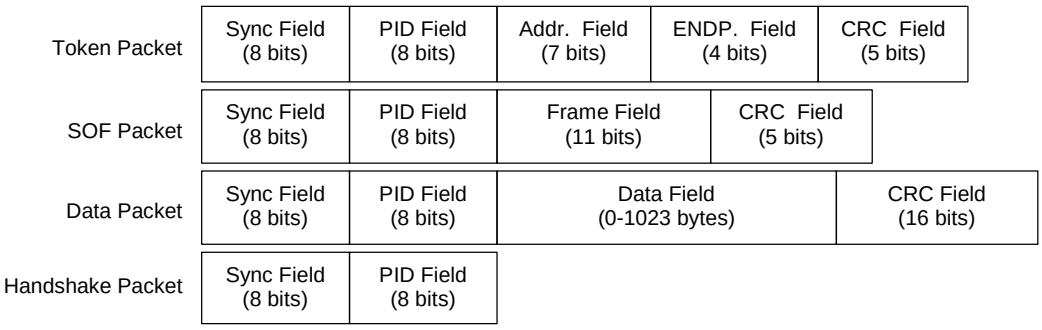


Figure 5-9. USB Packet Formats

Data is transferred LSb first. A cyclic redundancy check (CRC) is applied to all packets (except a handshake packet). A packet causing a CRC error is generally completely ignored by the receiver.

5.7.2 USB Programming

Programming the USB interface consists of configuration, which typically occurs during POST, and control, which occurs at runtime.

USB Configuration

Each USB controller functions as a PCI device within the 82801 component and is configured using PCI Configuration Registers as listed in Table 5-20.

NOTE:

Table 5-20.
USB Interface Configuration Registers

PCI Config. Address	Register	Reset Value	PCI Config. Address	Register	Reset Value
00, 01h	Vendor ID	8086h	0Eh	Header Type	00h
02, 03h	Device ID	[1]	20-23h	I/O Space Base Address	1d
04, 05h	PCI Command	0000h	2C, 2Dh	Sub. Vender ID	00h
06, 07h	PCI Status	0280h	3Ch	Interrupt Line	00h
08h	Revision ID	00h	3Dh	Interrupt Pin	03h
09h	Programming I/F	00h	60h	Serial Bus Release No.	10h
0Ah	Sub Class Code	03h	C0, C1h	USB Leg. Kybd./Ms. Cntrl.	2000h
0Bh	Base Class Code	0Ch	C4h	USB Resume Enable	00h

Note:

[1] USB 1.1 #1= 24D2h
USB 1.1 #2 = 24D4h
USB 1.1 #3 = 24D7h
USB 1.1 #4 = 24DDh
USB 2.0 = 24DDh

USB Control

The USB is controlled through I/O registers as listed in table 5-21.

Table 5-21.
USB Control Registers

I/O Address	Register	Default Value
00, 01h	Command	0000h
02, 03h	Status	0000h
04, 05h	Interupt Enable	0000h
06, 07	Frame Number	0000h
08, 0B	Frame List Base Address	0000h
0Ch	Start of Frame Modify	40h
10, 11h	Port 1 Status/Control	0080h
12, 13h	Port 2 Status/Control	0080h
18h	Test Data	00h

5.7.3 USB Connector

These systems provide type-A USB ports as shown in Figure 5-10 below.

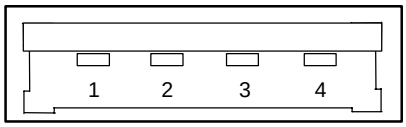


Figure 5-10. Universal Serial Bus Connector (Female)

Table 5-22.
USB Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	Vcc	+5 VDC	3	USB+	Data (plus)
2	USB-	Data (minus)	4	GND	Ground

5.7.4 USB Cable Data

The recommended cable length between the host and the USB device should be no longer than sixteen feet for full-channel (12 MB/s) operation, depending on cable specification (see following table).

Table 5-23.
USB Cable Length Data

Conductor Size	Resistance	Maximum Length
20 AWG	0.036 Ω	16.4 ft (5.00 m)
22 AWG	0.057 Ω	9.94 ft (3.03 m)
24 AWG	0.091 Ω	6.82 ft (2.08 m)
26 AWG	0.145 Ω	4.30 ft (1.31 m)
28 AWG	0.232 Ω	2.66 ft (0.81 m)

NOTE:

For sub-channel (1.5 MB/s) operation and/or when using sub-standard cable shorter lengths may be allowable and/or necessary.

The shield, chassis ground, and power ground should be tied together at the host end but left unconnected at the device end to avoid ground loops.

Color code	
Signal	**Insulation color**
Data +	Green
Data -	White
Vcc	Red
Ground	Black

5.8 Audio Subsystem

A block diagram of the audio subsystem is shown in Figure 5-11. These systems use the AC97 Audio Controller of the 82801 component to access and control an Analog Devices AD1981B Audio Codec, which provides the analog-to-digital (ADC) and digital-to-analog (DAC) conversions as well as mixing and equalizer functions. All control functions such as volume, audio source selection, and sampling rate are controlled through software through the AC97 Audio Controller of the 82801 ICH component. Control data and digital audio streams (record and playback) are transferred between the Audio Controller and the Audio Codec over the AC97 Link Bus. The codec mono analog output is applied to a single-channel amplifier that drives the internal speaker. Plugging headphones into the Headphone jack results in an active Spkr Mute signal used by the codec to ,silence the internal speaker

The analog interfaces allowing connection to external audio devices include:

Mic In—This input uses a three-conductor (stereo) mini-jack that is specifically designed for connection of a condenser microphone with an impedance of 10-K ohms. This is the default recording input after a system reset. On systems with both a front and rear microphone jack either jack is available for use (but not simultaneously).

Line In—This input uses a three-conductor (stereo) mini-jack that is specifically designed for connection of a high-impedance (10k-ohm) audio source such as a tape deck.

Headphones Out—This input uses a three-conductor (stereo) mini-jack that is designed for connecting a set of 16-ohm (nom.) stereo headphones or powered speakers. Plugging into the Headphones jack mutes the signal to the internal speaker and the Line Out jack as well.

Line Out—This output uses a three-conductor (stereo) mini-jack for connecting left and right channel line-level signals (20-K ohm impedance). A typical connection would be to a tape recorder's Line In (Record In) jacks, an amplifier's Line In jacks, or to powered speakers that contain amplifiers.

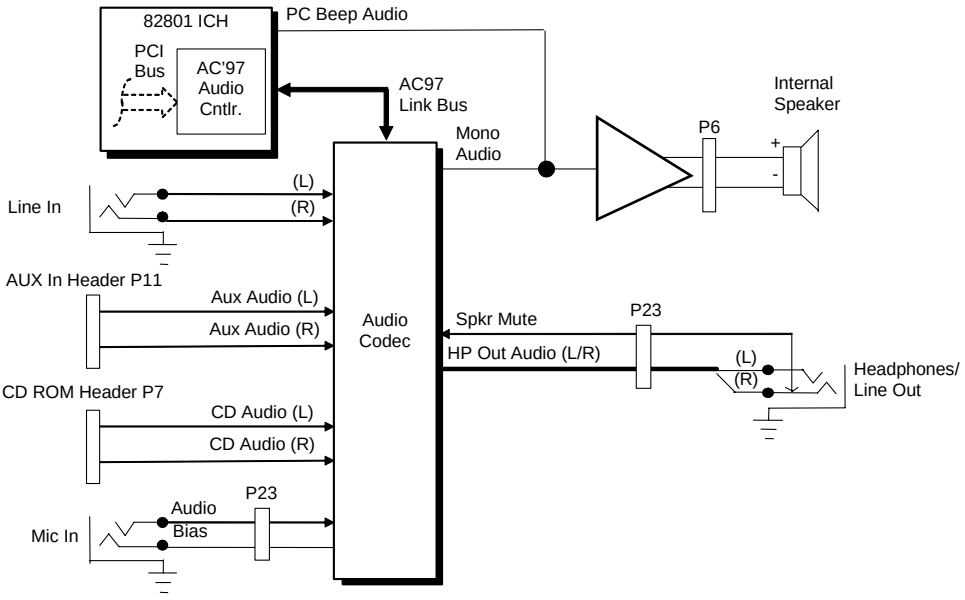


Figure 5-11. Audio Subsystem Functional Block Diagram

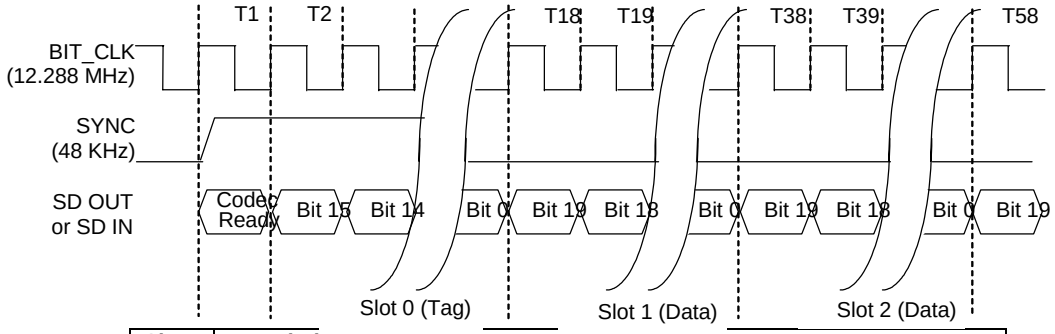
5.8.1 AC97 Audio Controller

The AC97 Audio Controller is a PCI device that is integrated into the 82801 ICH component and supports the following functions:

- Read/write access to audio codec registers
- 16-bit stereo PCM output @ up to 48 KHz sampling
- 16-bit stereo PCM input @ up to 48 KHz sampling
- Acoustic echo correction for microphone
- AC'97 Link Bus
- ACPI power management

5.8.2 AC97 Link Bus

The audio controller and the audio codec communicate over a five-signal AC97 Link Bus (Figure 5-12). The AC97 Link Bus includes two serial data lines (SD OUT/SD IN) that transfer control and PCM audio data serially to and from the audio codec using a time-division multiplexed (TDM) protocol. The data lines are qualified by a 12.288 MHz BIT_CLK signal driven by the audio codec. Data is transferred in frames synchronized by the 48-KHz SYNC signal, which is derived from the clock signal and driven by the audio controller. The SYNC signal is high during the frame's tag phase then falls during T17 and remains low during the data phase. A frame consists of one 16-bit tag slot followed by twelve 20-bit data slots. When asserted (typically during a power cycle), the RESET- signal (not shown) will reset all audio registers to their default values.



Slot	Description
0	Bit 15: Frame valid bit Bits 14-3: Slots 1-12 valid bits Bits 2-0: Codec ID
1	Command address: Bit 19, R/W; Bits 18..12, reg. Index; Bits 11..0, reserved.
2	Command data
3	Bits 19-4: PCM audio data, left channel (SD OUT, playback; SD IN, record) Bits 3-0 all zeros
4	Bits 19-4: PCM audio data, right channel (SD OUT, playback; SD IN, record) Bits 3-0 all zeros
5	Modem codec data (not used in this system)
6-11	Reserved
12	I/O control

Figure 5-12. AC97 Link Bus Protocol

5.8.3 Audio Codec

The audio codec provides pulse code modulation (PCM) coding and decoding of audio information as well as the selection and/or mixing of analog channels. As shown in Figure 5-13, analog audio from a microphone, tape, or CD can be selected and, if to be recorded (saved) onto a disk drive, routed through an analog-to-digital converter (ADC). The resulting left and right PCM record data are muxed into a time-division-multiplexed (TDM) data stream (SD IN signal) that is routed to the audio controller. Playback (PB) audio takes the reverse path from the audio controller to the audio codec as SD OUT data and is decoded and either routed through an equalizer or applied directly to the digital-to-analog converter (DAC). The codec supports simultaneous record and playback of stereo (left and right) audio. The Sample Rate Generator may be set for sampling frequencies up to 48 KHz.

The integrated analog mixer provides the computer control-console functionality handling multiple audio inputs.

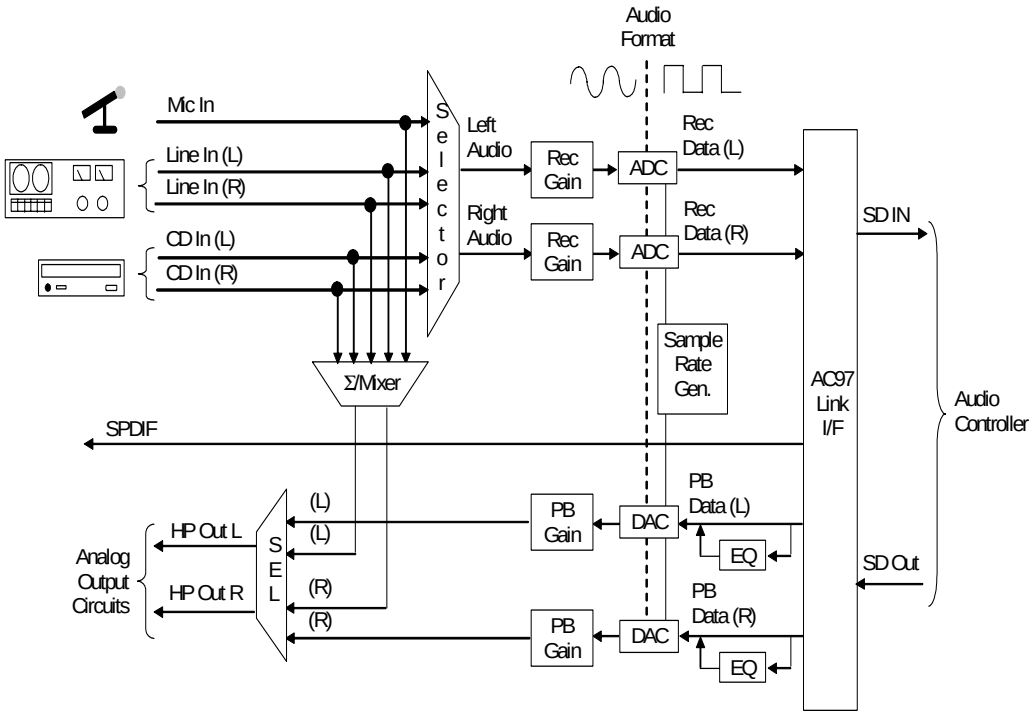


Figure 5-13. AD1981B Audio Codec Functional Block Diagram

All inputs and outputs are two-channel stereo except for the microphone input, which is inputted as a single-channel but mixed internally onto both left and right channels. The microphone input is the default active input. All block functions are controlled through index-addressed registers of the codec.

5.8.4 Audio Programming

Audio subsystem programming consists configuration, typically accomplished during POST, and control, which occurs during runtime.

Audio Configuration

The audio subsystem is configured according to PCI protocol through the AC97 audio controller function of the 82801 ICH. Table 5-24 lists the PCI configuration registers of the audio subsystem.

Table 5-24.
AC97 Audio Controller
PCI Configuration Registers (82801 Device 31/Function 5)

PCI Config. Address	Register	Value on Reset	PCI Config. Address	Register	Value on Reset
00-01h	Vendor ID	8086h	14-17h	Native Audio Bus Mstr. Addr.	1
02-03h	Device ID	24D5h	18-1Bh	Reserved	1h
04-05h	PCI Command	0000h	1C-2Bh	Reserved	1h
06-07h	PCI Status	0280h	2C-2Dh	Subsystem Vender ID	0000h
08h	Revision ID	XXh	2E-2Fh	Subsystem ID	0000h
09h	Programming	00h	30-3Bh	Reserved	--
0Ah	Sub-Class	01h	3Ch	Interrupt Line	00h
0Bh	Base Class Code	04h	3Dh	Interrupt Pin	02h
0Eh	Header Type	00h	3E-FFh	Reserved	0's
10-13h	Native Audio Mixer Base Addr.	1	--	--	--

Audio Control

The audio subsystem is controlled through a set of indexed registers that physically reside in the audio codec . The register addresses are decoded by the audio controller and forwarded to the audio codec over the AC97 Link Bus previously described. The audio codec's control registers (Table 5-25) are mapped into 64 kilobytes of variable I/O space.

Table 5-25.
AC97 Audio Codec Control Registers

Offset Address or Register	Value On Reset	Offset Address or Register	Value On Reset	Offset Address or Register	Value On Reset
00h Reset	0100h	14h Video Vol.	8808h	28h Ext. Audio ID.	0001h
02h Master Vol.	8000h	16h Aux Vol.	8808h	2Ah Ext. Audio Ctrl/Sts	0000h
04h Reserved	--	18h PCM Out Vol.	8808h	2Ch PCM DAC SRate	BB80h
06h Mono Mstr. Vol.	8000h	1Ah Record Sel.	0000h	32h PCM ADC SRate	BB80h
08h Reserved	--	1Ch Record Gain	8000h	34h Reserved	--
0Ah PC Beep Vol.	8000h	1Eh Reserved	--	72h Reserved	--
0Ch Phone In Vol.	8008h	20h Gen. Purpose	0000h	74h Serial Config.	7x0xh
0Eh Mic Vol.	8008h	22h 3D Control	0000h	76h Misc. Control Bits	0404h
10h Line In Vol.	8808h	24h Reserved	–	7Ch Vender ID1	4144h
12h CD Vol.	8808h	26h Pwr Mgnt.	000xh	7Eh Vender ID2	5340h

5.8.5 Audio Specifications

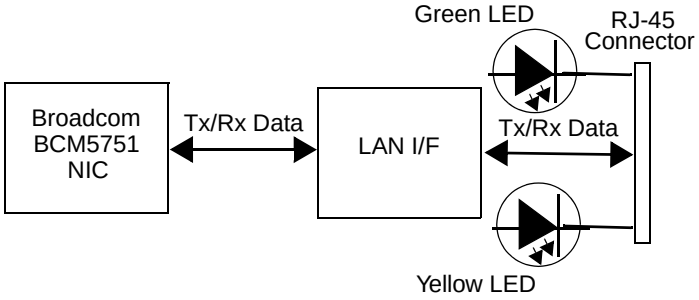
The specifications for the integrated AC97 audio subsystem are listed in Table 5-26.

Table 5-26.
AC97 Audio Subsystem Specifications

Parameter	Measurement
Sampling Rate	7040 KHz to 48 KHz
Resolution	16 bit
Nominal Input Voltage:	
Mic In (w/+20 db gain)	.283 Vp-p
Line In	2.83 Vp-p
Impedance:	
Mic In	1 K ohms (nom)
Line In	10 K ohms (min)
Line Out	800 ohms
Signal-to-Noise Ratio (input to Line Out)	90 db (nom)
Frequency Response (-3db to Line Output):	
Line Input	20 Hz – 20 KHz
Mic Input	100 Hz – 12 KHz
A/D (PC record)	
Line input	20 Hz – 19.2 KHz
Mic input	100 Hz – 8.8 Khz
D/A (PC playback)	20 Hz – 19.2 KHz
Max. Power Output (with 10% THD):	
Small Form Factor	8 watts (into 8 ohms)
Slim Desktop/Configurable Minitower	3 watts (into 16 ohms)
Input Gain Attenuation Range	-46.5 db
Master Volume Range	-94.5 db
Frequency Response:	
Codec	20–20 KHz
Speaker (Small Form Factor)	450–4000 Hz

5.9 Network Interface Controller

These systems provide 10/100/1000 Mbps network support through a Broadcom BCM5751 network interface controller (NIC), a PHY component, and a RJ-45 jack with integral status LEDs. The 82562-equivalent controller integrated into the 82801 ICH component is not used (disabled) in these systems. (Figure 5-14). The support firmware for the BCM5782 component is contained in the system (BIOS) ROM. The NIC can operate in half- or full-duplex modes, and provides auto-negotiation of both mode and speed. Half-duplex operation features an Intel-proprietary collision reduction mechanism while full-duplex operation follows the IEEE 802.3x flow control specification.



LED	Function
Green	Activity/Li nk. Indicates network activity and link pulse reception.
Yellow	Speed. Indicates link detection 100Mb/s mode.

Figure 5 14. Network Interface Controller Block Diagram

- The Network Interface Controller includes the following features:
- Dual high speed RISC controllers with 16-KB caches.
- Triple-mode support with auto-switching between 10BASE-T, 100BASE-TX, and 1000BASE-T.
- Power management support for ACPI 1.1, PXE 2.0, WOL, ASF 1.0, IPMI
- Cable testing capability
- Link and Activity LED indicator drivers

The controller features high and low priority queues and provides priority-packet processing for networks that can support that feature. The controller's micro-machine processes transmit and receive frames independently and concurrently. Receive runt (under-sized) frames are not passed on as faulty data but discarded by the controller, which also directly handles such errors as collision detection or data under-run.

The NIC uses 3.3 VDC auxiliary power, which allows the controller to support Wake-On-LAN (WOL) and Alert-On-LAN (AOL) functions while the main system is powered down.

For the features in the following paragraphs to function as described, the system unit must be plugged into a live AC outlet. Controlling unit power through a switchable power strip will, with the strip turned off, disable any wake, alert, or power mangement functionality.

5.9.1 Wake-On-LAN Support

The NIC supports the Wired-for-Management (WfM) standard of Wake-On-LAN (WOL) that allows the system to be booted up from a powered-down or low-power condition upon the detection of special packets received over a network. The NIC receives 3.3 VDC auxiliary power while the system unit is powered down in order to process special packets. The detection of a Magic Packet by the NIC results in the PME- signal on the PCI bus to be asserted, initiating system wake-up from an ACPI S1 or S3 state.

5.9.2 Alert Standard Format Support

Alert Standard Format (ASF) support allows the NIC to communicate the occurrence of certain events over a network to an ASF 1.0-compliant management console and, if necessary, take action that may be required. The ASF communications can involve the following:

- Alert messages sent by the client to the management console.
- Maintenance requests sent by the management console to the client.
- Description of client's ASF capabilities and characteristics.

The activation of ASF functionality requires minimal intervention of the user, typically requiring only booting a client system that is connected to a network with an ASF-compliant management console.

5.9.3 Power Management Support

The NIC features Wired-for-Management (WfM) support providing system wake up from network events (WOL) as well as generating system status messages (AOL) and supports ACPI power management environments. The controller receives 3.3 VDC (auxiliary) power as long as the system is plugged into a live AC receptacle, allowing support of wake-up events occurring over a network while the system is powered down or in a low-power state.

The Advanced Configuration and Power Interface (ACPI) functionality of system wake up is implemented through an ACPI-compliant OS and is the default power management mode. The following wakeup events may be individually enabled/disabled through the supplied software driver:

- Magic Packet—Packet with node address repeated 16 times in data portion

The following functions are supported in NDIS5 drivers but implemented through remote management software applications (such as LanDesk).

- Individual address match—Packet with matching user-defined byte mask
- Multicast address match—Packet with matching user-defined sample frame
- ARP (address resolution protocol) packet
- Flexible packet filtering—Packets that match defined CRC signature

The PROSet Application software (pre-installed and accessed through the System Tray or Windows Control Panel) allows configuration of operational parameters such as WOL and duplex mode.

5.9.4 NIC Programming

Programming the NIC consists of configuration, which occurs during POST, and control, which occurs at runtime. The Broadcom BCM5782 is configured as a PCI device and controlled through registers mapped in variable I/O space. The BIOS for the BCM5782 is contained within the HP/Compaq BIOS in system ROM. Refer to Broadcom documentation for details regarding BCM5782 register programming.

5.9.5 NIC Connector

Figure 5-14 shows the RJ-45 connector used for the NIC interface. This connector includes the two status LEDs as part of the connector assembly.

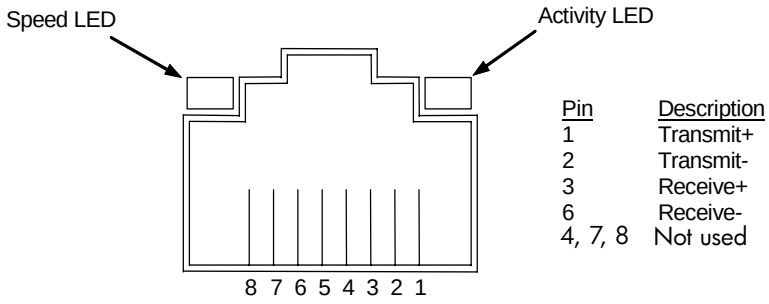


Figure 5 15. Ethernet TPE Connector (RJ-45, viewed from card edge)

5.9.6 NIC Specifications

Table 5-27.
NIC Specifications

Parameter	
Modes Supported	10BASE-T half duplex @ 10 Mb/s 10Base-T full duplex @ 20 Mb/s 100BASE-TX half duplex @ 100 Mb/s 100Base-TX full duplex @ 200 Mb/s 1000BASE-T half duplex @ 1 Gb/s 1000BASE-TX full duplex @ 2 Gb/s
Standards Compliance	IEEE 802.2 IEEE 802.3 & 802.3x IEEE Intel priority packet (801.1p)
OS Driver Support	MS-DOS MS Windows 3.1 MS Windows 95 (pre-OSR2), 98, and 2000 Professional, XP Home, XP Pro MS Windows NT 3.51 & 4.0 Novell Netware 3.x, 4.x, 5x Novell Netware/IntraNetWare SCO UnixWare 7 Linux 2.2, 2.4 PXE 2.0
Boot ROM Support	Intel PRO/100 Boot Agent (PXE 3.0, RPL)
F12 BIOS Support	Yes
Bus Inteface	PCI 2.2
Power Management Support	ACPI, PCI Power Management Spec.

6

Integrated Graphics Subsystem

6.1 Introduction

This chapter describes graphics subsystem that is integrated into the 82915G/GV GMCH component. This graphics subsystem employs the use of system memory to provide efficient, economical 2D and 3D performance.

The SFF, ST, MT, and CMT form factors may be upgraded by installing a graphics card into the PCI Express x16 or the PCI 2.3 slot. The USDT form factor may be upgraded by installing graphics card into the PCI 2.3 slot. An installed PCI Express or PCI 2.3 graphics controller card will be detected by the BIOS during the boot sequence and the integrated graphics controller of the 82915G GMCH will then be disabled (refer to section 6.5 for more information on upgrading the graphics subsystem).

This chapter covers the following subjects:

6.2 Functional Description

The Intel 915G/GV GMCH component includes an integrated graphics controller (IGC). (Figure 6-1). The IGC can directly drive an external, analog multi-scan monitor at resolutions up to and including 2048 x 1536 pixels. The IGC includes a memory management feature that allocates portions of system memory for use as the frame buffer and for storing textures and 3D effects.

The IGC provides two SDVO channels that are multiplexed through the PCI Express graphics interface. These SDVO ports may be used by an Advanced Digital Display (ADD2) card installed in the PCI Express graphics slot in driving two digital displays with a 200-megapixel clock. (NOTE: SDVO/ADD2 cards need to match the layout (normal or reversed) supported by the system board slot.)

The SSF, ST, MT, and CMT sytems may be upgraded by installing a separate PCI-E graphics card in the PCI Express x16 slot, which disables the onboard IGC. All systems may be also be upgraded by installing a PCI graphics card in the PCI 2.3 slot.

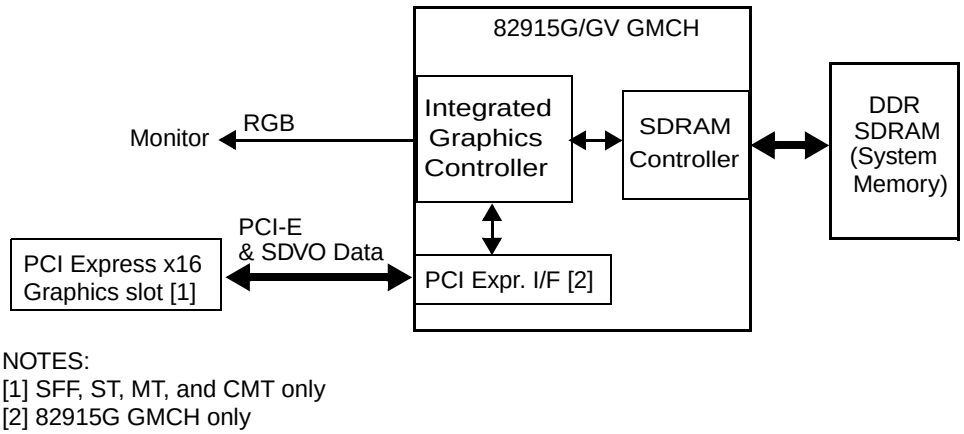


Figure 6-1. 915G-Based Graphics, Block diagram

The Integrated Graphics Controller provides the following functions:

- Rapid pixel and texel rendering using special pipelines that allow 2D and 3D operations to overlap, speeding up visual effects, reducing the amount of memory for texture storage.
- Zone rendering for optimizing 3D drawing, eliminating the need for local graphics memory by reducing the bandwidth.
- Dynamic video memory allocation, where the amount of memory required by the application is acquired (or released) by the controller.
- Intelligent memory management allowing tiled memory addressing, deep display buffering, and dynamic data management.
- Provides two serial digital video out (SDVO) channels for use by an appropriate ADD2 accessory card.

The graphics controller integrated into the 82915G/GV GMCH component includes 2D and 3D accelerator engines working with a deeply-pipelined pre-processor. Hardware cursor and overlay generators are also included as well as a legacy VGA processor core. The IGC supports three display devices:

- One progressive-scan analog monitor
- Up to two additional video displays with the installation of an optional Advanced Digital Display (ADD2) card in the PCI Express x16 graphics slot.

The IGC can support LVDS, TMDS, or TV output with the proper encoder option.

Special features of the integrated graphics controller include:

- 333-MHz core engine
- 400-MHz 24-bit RAMDAC
- 2D engine supporting GDI+, alpha stretch blithering, and color space conversion
- 3D engine supporting Z-bias and up to 1600 x 1200 w/32-bit color @ 85 hz refresh
- Video DVD support:

The Intel graphics controller uses a portion of system memory for instructions, textures, and frame (display) buffering. Using a process called Dynamic Video Memory Technology (DVMT), the controller dynamically allocates display and texture memory amounts according to the needs of the application running on the system.

6.2.1 Video Memory Allocation Reporting

The IGC does not have local memory at its disposal but instead uses a portion of system memory allocated for frame buffering and texturing. The total memory allocation is determined by the amount of system memory installed in a system. The video BIOS pre-allocates 8 megabytes of memory during POST. System memory that is pre-allocated is not seen by the operating system, which will report the total amount of memory installed less the amount of pre-allocated memory.

Example: A system with 128 MB of SDRAM with the video BIOS set to 8 MB will be reported by MS Windows as having 120 MB.

The IGC will use, in standard VGA/SVGA modes, pre-allocated memory as a true dedicated frame buffer. If the system boots with the OS loading the IGC Extreme Graphics drivers, the pre-allocated memory will then be re-claimed by the drivers and may or may not be used by the IGC in the “extended” graphic modes. However, it is important to note that pre-allocated memory is available only to the IGC, not to the OS.

The 915G's DVMT function is an enhancement over the Unified Memory Architecture (UMA) of earlier copyists. The DVMT of the 915G selects, during the boot process, the maximum graphics memory allocation possible according on the amount of system memory installed:

SDRAM Installed	Maximum Memory Allocation
128 to 256 megabytes	8-32 MB
257 to 511 megabytes	8-64 MB
> 512megabytes	8-128 MB

The actual amount of system memory used by the IGC (in the “extended” or “extreme” modes) will increase and decrease dynamically according to the needs of the graphics application. The amount of memory used solely for graphics (video) may be reported in a message on the screen, depending on the operating system and/or applications running on the machine.

For viewing the maximum amount of available frame buffer memory MS Windows 2000 or XP, go to Display Properties > Settings> Adapter.

The Microsoft Direct diagnostic tool included in most versions of Windows may be used to check the amount of video memory being used. The Display tab of the utility the “Approx. Total Memory” label will indicate the amount of video memory. The value will vary according to OS (Windows 98 will typically show 0.5 to 5 MB or higher, depending on screen resolution and application. In Windows 2000 or XP, the video memory size reported by DirectX will always be 32 MB, even if the total memory installed is over 128 MB.

Some applications, particularly games that require advanced 3D hardware acceleration, may not install or run correectly on systems using the IGC.

6.3 Display Modes

The IGC supports most standard display modes for 2D video displays up to and including 2048 x 1536 @ 85 Hz , and 3D display modes up to 1600 x 1200 @ 85 Hz. The highest resolution available will be determined by the following factors:

- Memory speed and amount
- Single or dual channel memory
- Number and type of monitors

The IGC is designed for optimum performance with multi-sync analog monitors. Digital displays may not provide an image as high in quality, depending on resolution.

6.4 Upgrading Graphics

The IGC of SFF, ST, MT, and CMT systems is upgradeable by installing an Advanced Digital Display 2 (ADD2) or a graphics controller card into the PCI Express x16 graphics slot. All systems can be upgraded by installing a PCI card in the PCI 2.3 slot (assuming no riser cards are installed). Depending on accessory, upgrading through the PCI Express x16 slot can provide digital monitor support and/or dual-monitor support allowing display-cloning or extended desktop functionality. Software drivers may need to be downloaded for specific cards.

Two SDVO channels are provided by the IGC for supporting two digital displays. Existing option cards and drivers support one CRT and digital display. Dual digital display support may be possible with future cards and drivers.

The upgrade procedure is as follows:

1. Shut down the system through the operating system.
2. Unplug the power cord from the rear of the system unit.
3. Remove the chassis cover.
4. Install the graphics card into the PCI Express x16 graphics or PCI 2.3 slot.
5. Replace the chassis cover.
6. Reconnect the power cord to the system unit.
7. Power up the system unit.

The BIOS will detect the presence of the PCI card and disable the IGC of the 82915G GMCH.

.If a PCI 2.3 graphics card is installed, the IGC can be re-enabled through the Setup Utility (F10) but may require driver installation. If a PCI-E graphics controller card is installed, the IGC cannot be enabled.

6.5 VGA Monitor Connector

These systems includes a standard VGA connector (Figure 6-3) for attaching an analog monitor:

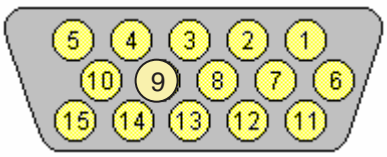


Figure 6 3. VGA Monitor Connector, (Female DB-15, as viewed from rear).

Table 6-1.
DB-15 Monitor Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	R	Red Analog	9	PWR	+5 VDC (fused) [1]
2	G	Blue Analog	10	GND	Ground
3	B	Green Analog	11	NC	Not Connected
4	NC	Not Connected	12	SDA	DDC2-B Data
5	GND	Ground	13	HSync	Horizontal Sync
6	R GND	Red Analog Ground	14	VSync	Vertical Sync
7	G GND	Blue Analog Ground	15	SCL	DDC2-B Clock
8	B GND	Green Analog Ground	--	--	--

NOTES:

[1] Fuse automatically resets when excessive load is removed.

7

Power and Signal Distribution

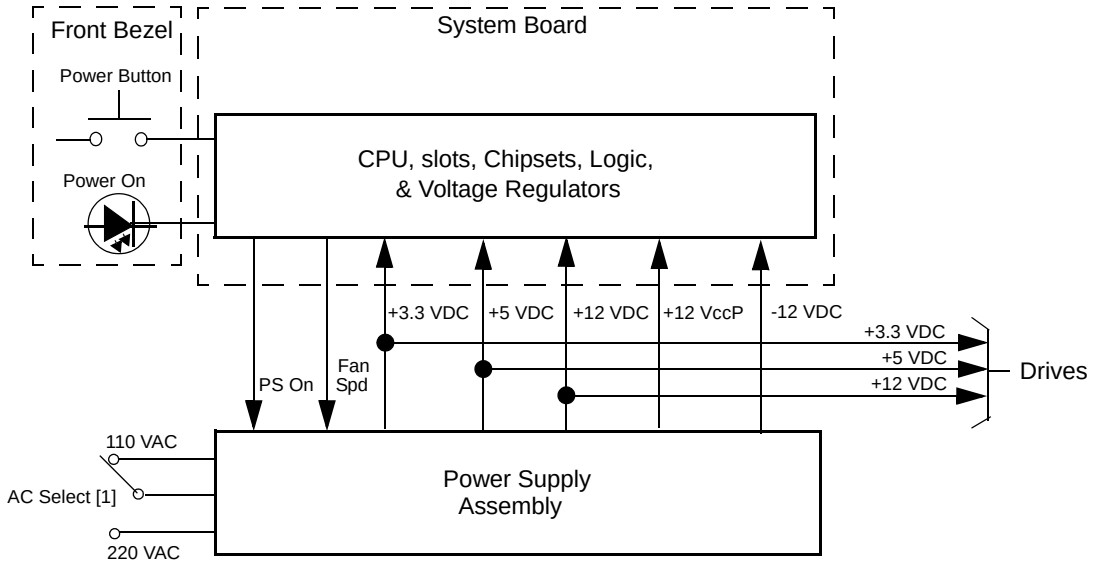
7.1 Introduction

This chapter describes the power supply and method of general power and signal distribution. Topics covered in this chapter include:

- Power supply assembly/control (7.2), page 7-1
- Power distribution (7.3), page 7-8
- Signal distribution (7.4), page 7-13

7.2 Power Supply Assembly/Control

These systems feature a power supply assembly that is controlled through programmable logic (Figure 7-1).



NOTE:
[1] 300-watt power supply only.

Figure 7-1. Power Distribution and Control, Block Diagram

7.2.1 Power Supply Assembly

These systems feature power supplies with power factor-correction logic. Four power supplies are used: a 200-watt power supply for the USDT unit, a 240-watt power supply for the SFF and ST units, a 300-watt power supply for the MT unit, and a 340-watt power supply for the CMT unit. All power supplies except that for the MT feature active power factor correction (PFC) and auto-ranging. The 300-watt power supply uses passive PFC and an AC select switch. Tables 7-1 through 7-4 list the specifications of the power supplies. Note that output load voltages are measured at the load-side of the output connectors.

Table 7-1.
200-Watt (USDT) Power Supply Assembly Specifications

	Range or Tolerance	Min. Current Loading [1]	Max. Current	Surge Current [2]	Max. Ripple
Input Line Voltage:					
115–230 VAC (auto-ranging)	90–264 VAC	--	--	--	--
Line Frequency	47–63 Hz	--	--	--	--
Input (AC) Current	--	--	4.0 A	--	--
+3.33 VDC Output	± 4 %	0.1 A	12.0 A	12.0 A	50 mV
+5.08 VDC Output	± 3.3 %	0.3 A	10.0 A	10.0 A	50 mV
+5.08 AUX Output	± 3.3 %	0.0 A	2.0 A	2.0 A	50 mV
+12 VDC Output [3]	± 5 %	0.1 A	15.5 A	18.0 A	120 mV
-12 VDC Output	± 10 %	0.0 A	0.15 A	0.15 A	200 mV

NOTES:

Total continuous power should not exceed 200 watts. Total surge power (<10 seconds w/duty cycle < 5 %) should not exceed 230 watts.

[1] Minimum loading requirements must be met at all times to ensure normal operation and specification compliance.

[2] Surge duration no longer than 10 seconds with 12-volt tolerance at +/- 10%.

[3] +12 VDC output can be split by the system board to +12 VDC (@ 3 A) and +12 Vcpu (@ 12.5 A) power planes.

Table 7-2.
240-Watt (SFF/ST) Power Supply Assembly Specifications

	Range/ Tolerance	Min. Current Loading [1]	Max. Current	Surge Current [2]	Max. Ripple
Input Line Voltage:					
115–230 VAC (auto-ranging)	90–264 VAC	--	--	--	--
Line Frequency	47–63 Hz	--	--	--	--
Input (AC) Current	--	--	5.0 A	--	--
+3.3 VDC Output	± 4%	0.1 A	19.0 A	19.0 A	50 mV
+5.08 VDC Output	± 3.3 %	0.3 A	14.0 A	14.0 A	50 mV
+5.08 AUX Output	± 3.3 %	0.0 A	3.0 A	3.0 A	50 mV
+12 VDC Output	± 5 %	0.1 A	7.5 A	9.0 A	120 mV
+12 VDC Output (Vcpu)	± 5 %	0.1 A	12.5 A	12.5 A	120 mv
-12 VDC Output	± 10 %	0.0 A	0.15 A	0.15 A	200 mV

NOTES:

Total continuous power should not exceed 240 watts. Total surge power (<10 seconds w/duty cycle < 5 %) should not exceed 260 watts.

[1] The minimum current loading figures apply to a PS On start up only.

Table 7-3.
300-Watt (MT) Power Supply Assembly Specifications

	Range/ Tolerance	Min. Current Loading [1]	Max. Current	Surge Current [2]	Max. Ripple
Input Line Voltage:					
115 VAC Setting	90 - 132 VAC	--	--	--	--
230 VAC Setting	180 - 264 VAC				
Line Frequency	47–63 Hz	--	--	--	--
Constant Input (AC) Current	--	--	8.0 / 4.0A	--	--
+3.3 VDC Output	± 5%	0.1 A	18.0 A	19.0 A	50 mV
+5 VDC Output	± 5%	0.3 A	25.0 A	25.0 A	50 mV
+5 AUX Output	± 5%	0.0 A	2.0 A	2.0 A	50 mV
+12 VDC Output	± 5 %	0.1 A	6.5 A	6.5 A	120 mV
+12 VDC Output (Vcpu)	± 5 %	0.1 A	12.5 A	12.5 A	120 mv
-12 VDC Output	± 10 %	0.0 A	0.8 A	0.8 A	200 mV

NOTES:

Total continuous power should not exceed 300 watts. Total continuous power (excluding 5 V aux output) should not exceed 290 watts

[1] Minimum loading requirements must be met at all times to ensure normal operation and specification compliance.

[2] Surge duration no longer than 10 seconds with 12-volt tolerance +/- 10%.

Table 7-4 lists the specifications for the 340-watt power supply used in the CMT form factor and in some MT form factors.

Table 7-4.
340-Watt (MT/CMT) Power Supply Assembly Specifications

	Range or Tolerance	Min. Current Loading [1]	Max. Current	Surge Current [2]	Max. Ripple
Input Line Voltage:					
115–230 VAC (auto-ranging)	90–132 VAC	--	--	--	--
Line Frequency	47–63 Hz	--	--	--	--
Input (AC) Current	--	--	6.0 A	--	--
+3.3 VDC Output	± 4 %	0.10 A	24.0 A	24.0 A	50 mV
+5.08 VDC Output	± 3.3 %	0.30 A	19.0 A	19.0 A	50 mV
+5.08 AUX Output	± 3.3 %	0.00 A	3.00 A	3.00 A	50 mV
+12 VDC Output	± 5 %	0.20 A	12.0 A	14.5 A	120 mV
+12 VDC Output (Vcpu)	± 5 %	0.00 A	12.5 A	12.5 A	200 mv
-12 VDC Output	± 10 %	0.00 A	0.15 A	0.15 A	200 mV

NOTES:

Total continuous output power should no exceed 340 watts. Maximum surge power should not exceed 360 watts. Total continuous power (excluding 5 V aux output) should not exceed 325watts.

Maximum combined power of +5 and +3.3 VDC is 160 watts.

[1] Minimum loading requirements must be met at all times to ensure normal operation and specification compliance.

[2] Surge duration no longer than 10 seconds with 12-volt tolerance +/- 10%.

7.2.2 Power Control

The power supply assembly is controlled digitally by the PS On signal (Figure 7-1). When PS On is asserted, the Power Supply Assembly is activated and all voltage outputs are produced. When PS On is de-asserted, the Power Supply Assembly is off and no voltages (except +5 AUX) are generated. Note that the +5 AUX voltages are always produced as long as the system is connected to a live AC source.

Power Button

The PS On signal is typically controlled through the Power Button which, when pressed and released, applies a negative (grounding) pulse to the power control logic. The resultant action of pressing the power button depends on the state and mode of the system at that time and is described as follows:

System State	Pressed Power Button Results In:
Off	Negative pulse, of which the falling edge results in power control logic asserting PS On signal to Power Supply Assembly, which then initializes. ACPI four-second counter is not active.
On, ACPI Disabled	Negative pulse, of which the falling edge causes power control logic to de-assert the PS On signal. ACPI four-second counter is not active.
On, ACPI Enabled	Pressed and Released Under Four Seconds: Negative pulse, of which the falling edge causes power control logic to generate SMI-, set a bit in the SMI source register, set a bit for button status, and start four-second counter. Software should clear the button status bit within four seconds and the Suspend state is entered. If the status bit is not cleared by software in four seconds PS On is de-asserted and the power supply assembly shuts down (this operation is meant as a guard if the OS is hung). Pressed and Held At least Four Seconds Before Release: If the button is held in for at least four seconds and then released, PS On is negated, de-activating the power supply.

Power LED Indications

A dual-color LED located on the front panel (bezel) is used to indicate system power status. The front panel (bezel) power LED provides a visual indication of key system conditions listed as follows:

Power LED	Condition
Steady green	Normal full-on operation
Blinks green @ 0.5 Hz	Suspend state (S1) or suspend to RAM (S3)
Blinks red 2 times @ 1 Hz [1]	Processor thermal shut down. Check air flow, fan operation, and CPU heat sink.
Blinks red 3 times @ 1 Hz [1]	Processor not installed. Install or reseat CPU.
Blinks red 4 times @ 1 Hz [1]	Power failure (power supply is overloaded). Check voltage selector (if applicable), stroage devices, expansion cards and/or system board.
Blinks red 5 times @ 1 Hz [1]	Pre-video memory error. Incompatible or incorrectly seated DIMM.
Blinks red 6 times @ 1 Hz [1]	Pre-video graphics error. On system with integrated graphics, check/replace system board. On system with graphics card, check/replace graphics card.
Blinks red 7 times @ 1 Hz [1]	PCA failure. Check/replace system board.
Blinks red 8 times @ 1 Hz [1]	Invalid ROM (checksum error). Reflash ROM using ROMPaq diskette or replace system board.
Blinks red 9 times @ 1 Hz [1]	System powers on but fails to boot. Check power supply, CPU, system board.
Blinks red 10 times @ 1 Hz [1]	Bad option card.
No light	System dead. Press and hold power button for **less** than 4 seconds. If HD LED turns green then check voltage select switch setting or expansion cards. If no LED light then check power button/power supply cables to system board or system board.

NOTE:

[1] Will be accompanied by the same number of beeps, with 2-second pause between cycles. Beeps stop after 5 cycles.

Wake Up Events

The PS On signal can be activated with a power “wake-up” of the system due to the occurrence of a magic packet, serial port ring, or PCI power management (PME) event. These events can be individually enabled through the Setup utility to wake up the system from a sleep (low power) state.

Wake-up functionality requires that certain circuits receive auxiliary power while the system is turned off. The system unit must be plugged into a live AC outlet for wake up events to function. Using an AC power strip to control system unit power will disable wake-up event functionality.

The wake up sequence for each event occurs as follows:

Wake-On-LAN

The network interface controller (NIC) can be configured for detection of a “Magic Packet” and wake the system up from sleep mode through the assertion of the PME- signal on the PCI bus. Refer to Chapter 5, “Network Support” for more information.

Modem Ring

A ring condition on a serial port can be detected by the power control logic and, if so configured, cause the PS On signal to be asserted.

Power Management Event

A power management event that asserts the PME- signal on the PCI bus can be enabled to cause the power control logic to generate the PS On. Note that the PCI card must be PCI ver. 2.2 compliant to support this function.

7.2.3 Power Management

These systems include power management functions designed to conserve energy. These functions are provided by a combination of hardware, firmware (BIOS) and software. The system provides the following power management features:

- ACPI v1.0b compliant (ACPI modes C1, C2, S1, and S3,)
- APM 1.2 compliant
- U.S. EPA Energy Star compliant

Table 7-5 shows the comparison in power states.

Table 7-5.
System Power States

Power State	System Condition	Power Consumption	Transition To S0 by [2]	OS Restart Required
G0, S0, D0	System fully on. OS and application is running, all components.	Maximum	N/A	No
G1, S1, C1, D1	System on, CPU is executing and data is held in memory. Some peripheral subsystems may be on low power. Monitor is blanked.	Low	< 2 sec after keyboard or pointing device action	No
G1, S2/3, C2, D2 (Standby/or suspend)	System on, CPU not executing, cache data lost. Memory is holding data, display and I/O subsystems on low power.	Low	< 5 sec. after keyboard, pointing device, or power button action	No
G1, S4, D3 (Hibernation)	System off. CPU, memory, and most subsystems shut down. Memory image saved to disk for recall on power up.	Low	<25 sec. after power button action	Yes
G2, S5, $D3_{cold}$	System off. All components either completely shut down or receiving minimum power to perform system wake-up.	Minimum	<35 sec. after power button action	Yes
G3	System off (mechanical). No power to any internal components except RTC circuit. [1]	None	—	—

NOTES:

Gn = Global state.

Sn = Sleep state.

Cn = ACPI state.

Dn = PCI state.

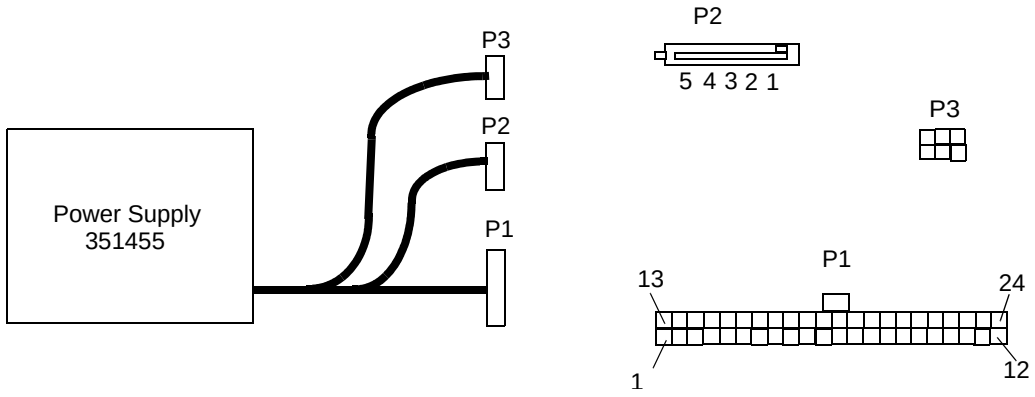
[1] Power cord is disconnected for this condition.

[2] Actual transition time dependent on OS and/or application software.

7.3 Power Distribution

7.3.1 3.3/5/12 VDC Distribution

The power supply assembly includes a multi-connector cable assembly that routes +3.3 VDC, +5 VDC, +5 VDC STB, +12 VC, and -12 VDC to the system board as well as to the individual drive assemblies. Figure 7-2 shows the power supply cabling for the Ultra Slim Desktop form factor.

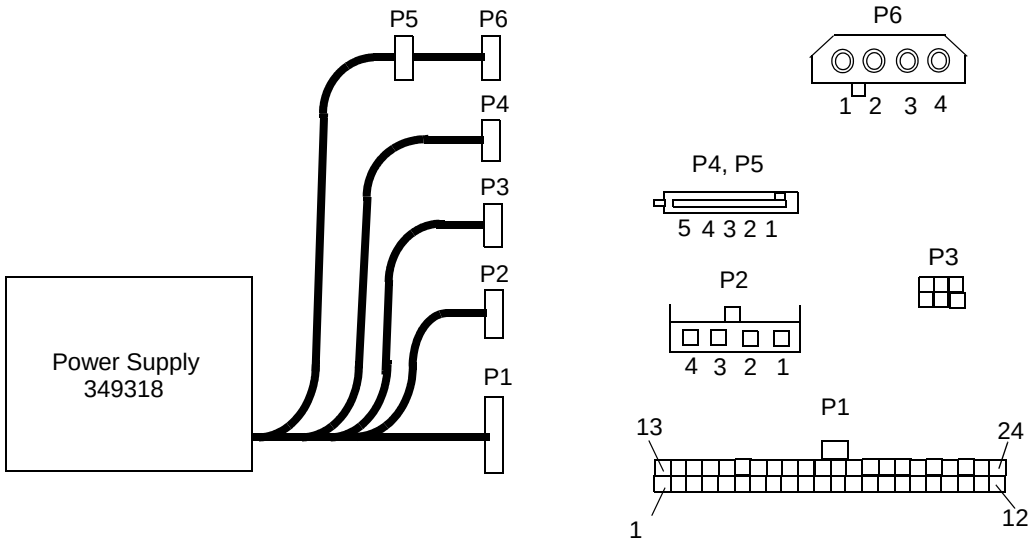


Conn	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 12
P1	+5 aux	RTN	+ 5	+5	PS On	RTN	Pwr Gd	+3.3	+3.3	Tach	RTN	Fan
P1 [1]	+12	+5 sns	RTN	+5	+5	+3.3	RTN	+3.3 sns	+3.3	+3.3	RTN	-12
P2	+3.3	RTN	+5	RTN	+12							
P3	RTN	RTN	RTN	VccP	VccP	+12						

NOTES:
Connectors not shown to scale.
All + and – values are VDC.
RTN = Return (signal ground)
sns = sense
GND = Power ground
RS = Remote sense
FO = Fan off
FSpd = Fan speed
FS = Fan Sink
FC = Fan Command
Vccp = +12 VDC for CPU
[1] This row represents pins 13 – 24 of connector P1.

Figure 7-2. USDT Power Cable Diagram

Figure 7-3 shows the power supply cabling for the SFF/ST systems.

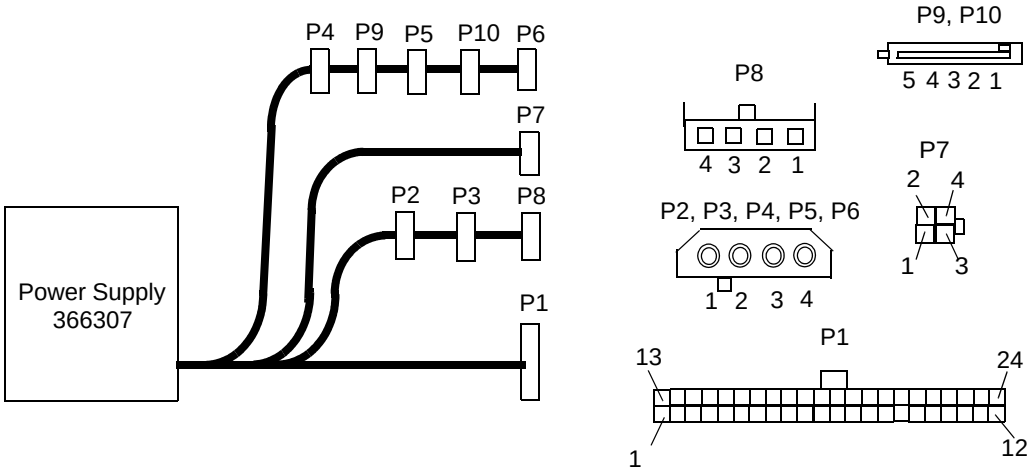


Conn	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 12
P1	+5 aux	RTN	+ 5	+5	PS On	RTN	Pwr Gd	+3.3	+3.3	Tach	RTN	Fan
P1 [1]	+12	+5 sns	RTN	+5	+5	+3.3	RTN	+3.3 sns	+3.3	+3.3	RTN	-12
P2	+5	RTN	RTN	+12								
P3	RTN	RTN	RTN	VccP	VccP	+12						
P4, 5	+3.3	RTN	+5	RTN	+12							
P6	+12	RTN	RTN	+5								

Connectors not shown to scale.
All + and - values are VDC.
RTN = Return (signal ground)
sns = sense
GND = Power ground
RS = Remote sense
FC = Fan command
FO = Fan off
FSpd = Fan speed
FS = Fan Sink
POK = Power OK (power good)
VccP = +12 for CPU
[1] This row represents pins 13–24 of connector P1

Figure 7-3. SFF/ST Power Cable Diagram

Figure 7-4 shows the power supply cabling for the microtower systems.



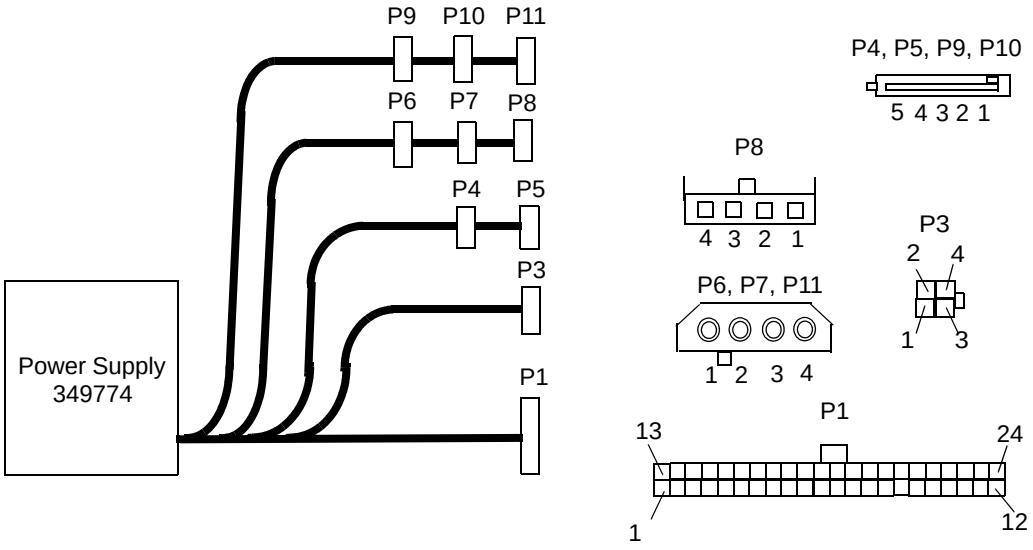
Conn	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 12
P1	+3.3RS	+3.3	RTN	+5	RTN	+5	RTN	POK	5 aux	+12	+12	+3.3
P1 [1]	+3.3	-12	RTN	PS On	RTN	RTN	RTN	Open	+5	+5	+5	RTN
P2-6	+12	RTN	RTN	+5								
P7	RTN	RTN	+12	+12								
P8	+5	RTN	RTN	+12								
P9, 10	+3.3	RTN	+5	RTN	+12							

NOTES:

Connectors not shown to scale.
All + and - values are VDC.
RTN = Return (signal ground)
GND = Power ground
RS = Remote sense
POK = Power ok (power good)
FC = Fan Command
[1] This row represents pins 13–24 of connector P1.

Figure 7-4. MT Power Cable Diagram

Figure 7-4 shows the power supply cabling for the convertible minitower systems.



Conn	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 12
P1	+3.3	+3.3	RTN	+5	RTN	+5	RTN	POK	5 aux	+12	+12	+3.3
P1 [1]	RS	-12	RTN	PS On	RTN	RTN	RTN	Open	+5	+5	+5	RTN
P3	RTN	RTN	VccP	VccP								
P4, 5, 9, 10	+3.3	RTN	+5.08	RTN	+12							
P6, 7, 11	+12	RTN	RTN	+5								
P8	+5	RTN	RTN	+12								

NOTES:

Connectors not shown to scale.
All + and - values are VDC.
RTN = Return (signal ground)
GND = Power ground
RS = Remote sense
POK = Power ok (power good)
FC = Fan Command
[1] This row represents pins 13–24 of connector P1.

Figure 7-5. CMT Power Cable Diagram

The 340-watt power supply is also used on some MT SKUs..

7.3.2 Low Voltage Production/Distribution

Auxiliary voltages less than 5 volts and all voltages less than 3.3 volts are produced through regulator circuitry (Figure 7-6) on the system board.

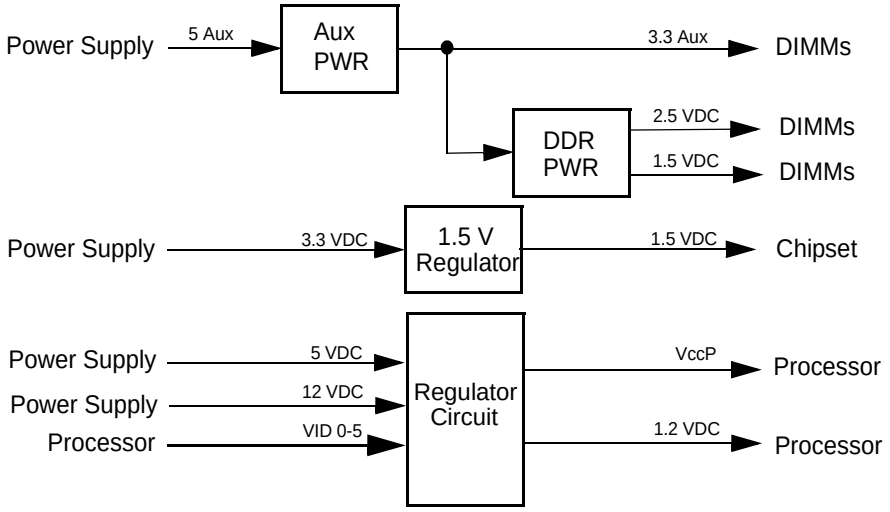
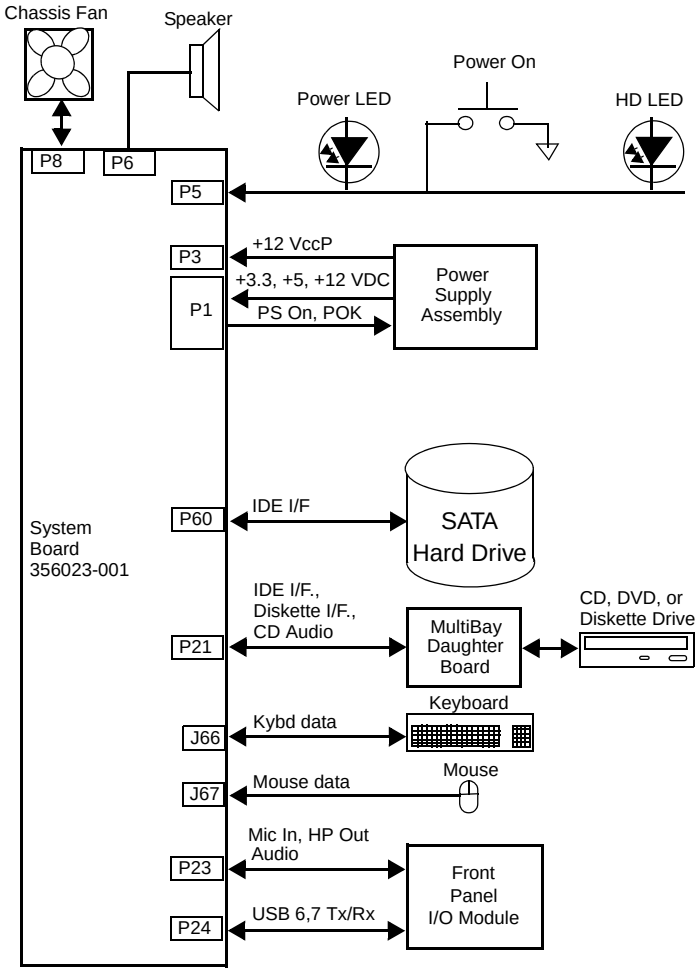


Figure 7-6. Low Voltage Supply and Distribution Diagram

The VccP regulator produces the VccP (processor core) voltage according to the strapping of signals VID0..5 by the processor and may range from 0.8375 to 1.6 VDC.

7.4 Signal Distribution

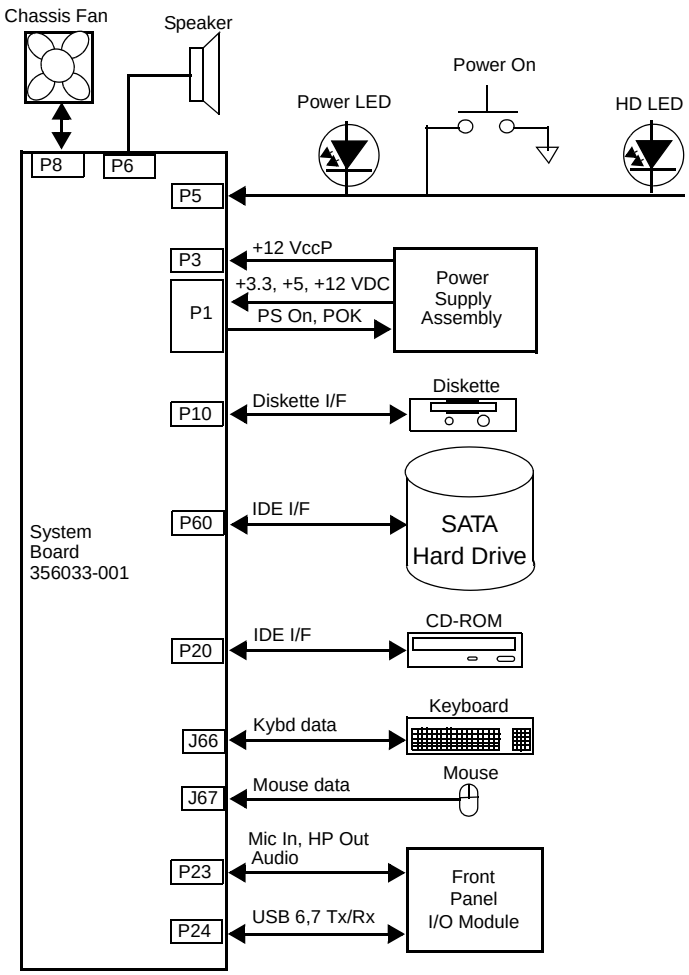
Figures 7-7 through 7-9 show general signal distribution between the main subassemblies of the system units.



NOTES:

See Figure 7-10 for header pinout.

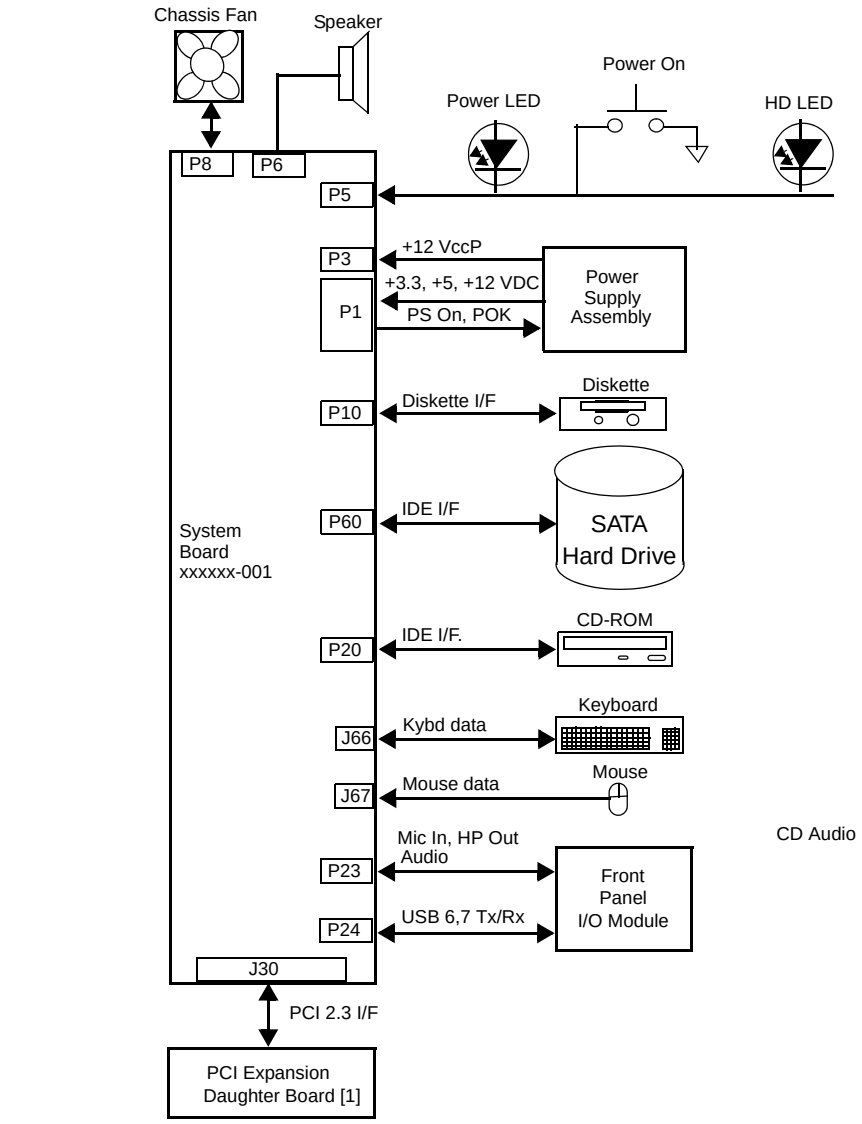
Figure 7-7. USDT Form Factor Signal Distribution Diagram



NOTES:

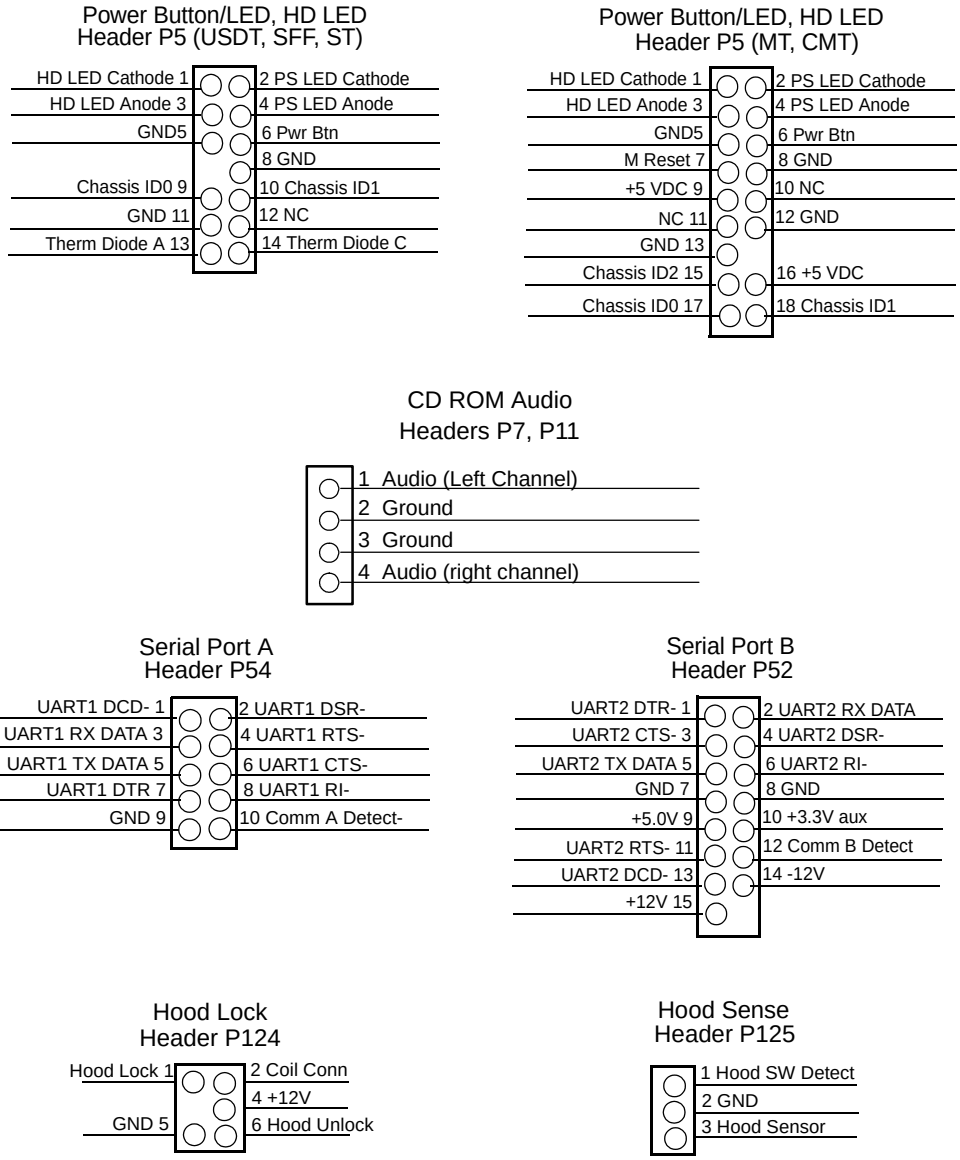
See Figure 7-7 for header pinout.

Figure 7-8. SFF / ST Form Factor Signal Distribution Diagram



Notes:
[1] Applicable to CMT form factor only.

Figure 7-9. MT / CMT Form Factor Signal Distribution Diagram



NOTE:

No polarity consideration required for connection to speaker header P6.

Figure 7-10. Header Pinouts

8

BIOS ROM

8.1 Introduction

The Basic Input/Output System (BIOS) of the computer is a collection of machine language programs stored as firmware in read-only memory (ROM). The BIOS ROM includes such functions as Power-On Self Test (POST), PCI device initialization, Plug 'n Play support, power management activities, and the Setup utility. The firmware contained in the BIOS ROM supports the following operating systems and specifications:

- DOS 6.2
- Windows 3.1 (and Windows for Workgroups 3.11)
- Windows 95, 98SE, 2000, XP Professional, and XP Home
- Windows NT 4.0 (SP6 required for PnP support)
- OS/2 ver 2.1 and OS/2 Warp
- SCO Unix
- DMI 2.1
- Intel Wired for Management (WfM) ver. 2.2
- Alert-On-LAN (AOL) and Wake-On-LAN (WOL)
- ACPI and OnNow
- SMBIOS 2.3.1
- PC98/99/00 and NetPC
- Intel PXE boot ROM for the integrated LAN controller
- BIOS Boot Specification 1.01
- Enhanced Disk Drive Specification 3.0
- “El Torito” Bootable CD-ROM Format Specification 1.0
- ATAPI Removeable Media Device BIOS Specification 1.0

The BIOS ROM is a 512KB Intel Firmware Hub (or Firmware Hub-compatible) part. The runtime portion of the BIOS resides in a 128KB block from E0000h to FFFFFh.

This chapter includes the following topics:

8.2 ROM Flashing

The system BIOS firmware is contained in a flash ROM device that can be re-written with BIOS code (using the ROMPAQ utility or a remote flash program) allowing easy upgrading, including changing the splash screen displayed during the POST routine.

8.2.1 Upgrading

Upgrading the BIOS is not normally required but may be necessary if changes are made to the unit's operating system, hard drive, or processor. All BIOS ROM upgrades are available directly from HP. Flashing is done either locally with the HP-provided Windows program, a ROMPaq diskette or remotely using the network boot function (described in the section 8.3.2).

This system includes 64 KB of write-protected boot block ROM that provides a way to recover from a failed flashing of the system BIOS ROM. If the BIOS ROM fails the flash check, the boot block code provides the minimum amount of support necessary to allow booting the system from the diskette drive and re-flashing the system ROM with a ROMPAQ diskette. Note that if an administrator password has been set in the system the boot block will prompt for this password by illuminating the caps lock keyboard LED and displaying a message if video support is available. A PS/2 keyboard must be used during bootblock operation.

Since video may not be available during the initial boot sequence the boot block routine uses the Num Lock, Caps Lock, and Scroll Lock LEDs of the PS/2 keyboard to communicate the status of the ROM flash as follows:

Table 8-1
Boot Block Codes

Num Lock LED	Cap Lock LED	Scroll Lock LED	Meaning
Off	On	Off	Administrator password required.
On	Off	Off	Boot failed. Reset required for retry.
Off	Off	On	Flash failed.
On	On	On	Flash complete.

8.2.2 Changeable Splash Screen

A corrupted splash screen may be restored by the user with the ROMPAQ software. Depending on the system, changing (customizing) the splash screen may only be available with asistance from HP.

The splash screen (image displayed during POST) is stored in the BIOS ROM and may be replaced with another image of choice by using the Image Flash utility (Flashi.exe). The Image Flash utility allows the user to browse directories for image searching and pre-viewing. Background and foreground colors can be chosen from the selected image's palette.

The splash screen image requirements are as follows:

- Format = Windows bitmap with 4-bit RLE encoding
- Size = 424 (width) x 320 (height) pixels
- Colors = 16 (4 bits per pixel)
- File Size = < 64 KB

The Image Flash utility can be invoked at a command line for quickly flashing a known image as follows:

```
>\Flashi.exe [Image_Filename] [Background_Color] [Foreground_Color]
```

The utility checks to insure that the specified image meets the splash screen requirements listed above or it will not be loaded into the ROM.

8.3 Boot Functions

The BIOS supports various functions related to the boot process, including those that occur during the Power On Self-Test (POST) routine.

8.3.1 Boot Device Order

The default boot device order is as follows:

1. IDE CD-ROM drive (EL Torito CD images)
2. Diskette drive (A:)
3. MultiBay device (A: or CD-ROM) if applicable
4. USB device
5. Hard drive (C:)
6. Network interface controller

The order can be changed in the ROM-based Setup utility (accessed by pressing F10 when so prompted during POST). The options are displayed only if the device is attached, except for USB devices. The USB option is displayed even if no USB storage devices are present. The hot IPL option is available through the F9 utility, which allows the user to select a hot IPL boot device.

8.3.2 Network Boot (F12) Support

The BIOS supports booting the system to a network server. The function is accessed by pressing the F12 key when prompted at the lower right hand corner of the display during POST. Booting to a network server allows for such functions as:

- Flashing a ROM on a system without a functional operating system (OS).
- Installing an OS.
- Installing an application.

These systems include, as standard, an integrated Intel 82562-equivalent NIC with Preboot Execution Environment (PXE) ROM and can boot with a NetPC-compliant server.

8.3.3 Memory Detection and Configuration

This system uses the Serial Presence Detect (SPD) method of determining the installed DIMM configuration. The BIOS communicates with an EEPROM on each DIMM through the SMBus to obtain data on the following DIMM parameters:

- Presence
- Size
- Type
- Timing/CAS latency
- PC133 capability

Refer to Chapter 3, “Processor/Memory Subsystem” for the SPD format and DIMM data specific to this system.

The BIOS performs memory detection and configuration with the following steps:

1. Program the buffer strength control registers based on SPD data and the DIMM slots that are populated.
2. Determine the common CAS latency that can be supported by the DIMMs.
3. Determine the memory size for each DIMM and program the GMCH accordingly.
4. Enable refresh

8.3.4 Boot Error Codes

The BIOS provides visual and audible indications of a failed system boot by using the LEDS on the PS/2 keyboard and the system board speaker. The error conditions are listed in the following table.

Table 8-2
Boot Error Codes

Visual [1]	Audible	Meaning
Num Lock LED blinks	1 short, 2 long beeps	System memory not present or incompatible.
Scroll Lock LED blinks	2 long, 1 short beeps	Hardware failure before graphics initialization.
Caps Lock LED blinks	1 long, 2 short beeps	Graphics controller not present or failed to initialize.
Num, Caps, Scroll Lock LEDs blink	1 long, 3 short beeps	ROM failure.
Num, Caps, Scroll Lock LEDs blink in sequence	none	Network service mode

NOTE:

[1] Provided with PS/2 keyboard only.

8.4 Setup Utility

The Setup utility (stored in ROM) allows the user to configure system functions involving security, power management, and system resources. The Setup utility is ROM-based and invoked when the **F10** key is pressed and held during the computer boot cycle. Highlights of the Setup utility are described in the following table.

After pressing and releasing the computer's power button, press and hold the F10 key until the Setup Utility screen is displayed.

Table 8-3
Setup Utility

Heading	Option	Description
File	System Information	Lists: • Product name • Processor type/speed/stepping • Cache size (L1/L2) • Installed memory size/speed, number of channels (single or dual) (if applicable) • Integrated MAC address for embedded, enabled NIC (if applicable) • System ROM (includes family name and version) • Chassis serial number • Asset tracking number
	About	Displays copyright information.
	Set Time and Date	Allows you to set system time and date.
	Replicated Setup	**Save to Removable Media** Saves system configuration, including CMOS, to a formatted 1.44-MB diskette, a USB flash media device, or a diskette-like device (a storage device set to emulate a diskette drive). **Restore from Removable Media** Restores system configuration from a diskette, a USB flash media device, or a diskette-like device.
	Default Setup	**Save Current Settings as Default** Saves the current system configuration settings as the default. **Restore Factory Settings as Default** Restores the factory system configuration settings as the default.
	Apply Defaults and Exit	Applies the currently selected default settings and clears any established passwords.
	Ignore Changes and Exit	Exits Computer Setup without applying or saving any changes.

Support for specific Computer Setup options may vary depending on the hardware configuration.

Table 8-3
Setup Utility

Heading	Option	Description
File *(continued)*	Save Changes and Exit	Saves changes to system configuration or default settings and exits Computer Setup.
Storage	Device Configuration	Lists all installed BIOS-controlled storage devices. When a device is selected, detailed information and options are displayed. The following options may be presented.
		Diskette Type Identifies the highest capacity media type accepted by the diskette drive. Legacy Diskette Drives Options are 3.5" 1.44 MB and 5.25" 1.2 MB.
		Drive Emulation Allows you to select a drive emulation type for a certain storage device. (For example, a Zip drive can be made bootable by selecting diskette emulation.)

Drive Type	Emulation Options
ATAPI Zip drive	None (treated as Other)
	Diskette (treated as diskette drive)
ATA Hard disk	None (treated as Other)
	Disk (treated as hard drive)
Legacy diskette	No emulation options available
CD-ROM drive	No emulation options available
ATAPI LS-120	None (treated as Other).
	Diskette (treated as diskette drive).

	Default Values IDE/SATA
	Multisector Transfers *(ATA disks only)* Specifies how many sectors are transferred per multi-sector PIO operation. Options (subject to device capabilities) are Disabled, 8, and 16.
	⚠ **CAUTION:** Ordinarily, the translation mode selected automatically by the BIOS should not be changed. If the selected translation mode is not compatible with the translation mode that was active when the disk was partitioned and formatted, the data on the disk will be inaccessible.

✎ Support for specific Computer Setup options may vary depending on the hardware configuration.

Table 8-3
Setup Utility

Heading	Option	Description
		Translation Parameters (ATA disks only) This feature appears only when User translation mode is selected. Allows you to specify the parameters (logical cylinders, heads, and sectors per track) used by the BIOS to translate disk I/O requests (from the operating system or an application) into terms the hard drive can accept. Logical cylinders may not exceed 1024. The number of heads may not exceed 256. The number of sectors per track may not exceed 63. These fields are only visible and changeable when the drive translation mode is set to User.
	Storage Options	**Removable Media Boot** Enables/disables ability to boot the system from removable media.
		Legacy Diskette Write Enables/disables ability to write data to legacy diskettes. After saving changes to Removable Media Write, the computer will restart. Turn the computer off, then on, manually.
		BIOS DMA Data Transfers Allows you to control how BIOS disk I/O requests are serviced. When "Enable" is selected, the BIOS will service ATA disk read and write requests with DMA data transfers. When "Disable" is selected, the BIOS will service ATA disk read and write requests with PIO data transfers.
		SATA Emulation Allows you to choose how the SATA controller and devices are accessed by the operating system. "Separate IDE Controller" is the default option. Up to 4 SATA and 2 PATA devices may be accessed in this mode. The SATA and PATA controllers appear as two separate IDE controllers. Use this option with Microsoft Windows 2000 and Windows XP. • SATA 0 is seen as SATA Primary Device 0 • SATA 1 (if present) is seen as SATA Secondary Device 0 "Combined IDE Controller" is the other option. Up to 2 PATA and 2 SATA devices may be accessed in this mode. The SATA and PATA controllers appear as one combined IDE controller. Use this option with Microsoft Windows 98 and earlier operating systems. • PATA Primary Device 0 replaces SATA 1 • PATA Primary Device 1 replaces SATA 3
		IDE Controller Allows you to enable or disable the primary IDE controller. This feature is supported on select models only.
		Primary SATA Controller Allows you to enable or disable the Primary SATA controller.

Support for specific Computer Setup options may vary depending on the hardware configuration.

Table 8-3
Setup Utility

Heading	Option	Description
		Secondary SATA Controller Allows you to enable or disable the Secondary SATA controller. This feature is supported on select models only.
	DPS Self-Test	Allows you to execute self-tests on ATA hard drives capable of performing the Drive Protection System (DPS) self-tests. This selection will only appear when at least one drive capable of performing the DPS self-tests is attached to the system.
Storage *(continued)*	Boot Order	Allows you to: • Specify the order in which attached devices (such as a USB flash media device, diskette drive, hard drive, optical drive, or network interface card) are checked for a bootable operating system image. Each device on the list may be individually excluded from or included for consideration as a bootable operating system source. • Specify the order of attached hard drives. The first hard drive in the order will have priority in the boot sequence and will be recognized as drive C (if any devices are attached). MS-DOS drive lettering assignments may not apply after a non-MS-DOS operating system has started. **Shortcut to Temporarily Override Boot Order** To boot **one time** from a device other than the default device specified in Boot Order, restart the computer and press **F9** when the monitor light turns green. After POST is completed, a list of bootable devices is displayed. Use the arrow keys to select the preferred bootable device and press **Enter**. The computer then boots from the selected non-default device for this one time.
Security	Setup Password	Allows you to set and enables setup (administrator) password. If the setup password is set, it is required to change Computer Setup options, flash the ROM, and make changes to certain plug and play settings under Windows. See the *Troubleshooting Guide* on the *Documentation CD* for more information.
	Power-On Password	Allows you to set and enable power-on password. See the *Troubleshooting Guide* for more information.
	Password Options (This selection will appear only if a power-on password is set.)	Allows you to specify whether the password is required for warm boot (**CTRL+ALT+DEL**). See the *Desktop Management Guide* for more information.

Support for specific Computer Setup options may vary depending on the hardware configuration.

Table 8-3
Setup Utility

Heading	Option	Description
	Smart Cover	Allows you to: • Lock/unlock the Cover Lock. • Set the Cover Removal Sensor to Disable/Notify User/Setup Password. *Notify User* alerts the user that the sensor has detected that the cover has been removed. *Setup Password* requires that the setup password be entered to boot the computer if the sensor detects that the cover has been removed. This feature is supported on select models only. See the *Desktop Management Guide* on the *Documentation CD* for more information.
Security *(continued)*	Embedded Security	Allows you to: • Enable/disable the Embedded Security device. • Reset the device to Factory Settings. This feature is supported on select models only. See the *Desktop Management Guide* on the *Documentation CD* for more information.
	Device Security	Enables/disables serial ports, parallel port, front USB ports, system audio, network controllers (some models), MultiBay devices (some models), SMBus controller (some models), and SCSI controllers (some models).
	Network Service Boot	Enables/disables the computer's ability to boot from an operating system installed on a network server. (Feature available on NIC models only; the network controller must reside on the PCI bus or be embedded on the system board.)
	System IDs	Allows you to set: • Asset tag (18-byte identifier) and ownership Tag (80-byte identifier displayed during POST). See the *Desktop Management Guide* on the *Documentation CD* for more information. • Chassis serial number or Universal Unique Identifier (UUID) number. The UUID can only be updated if the current chassis serial number is invalid. (These ID numbers are normally set in the factory and are used to uniquely identify the system.) • Keyboard locale setting (for example, English or German) for System ID entry.

Support for specific Computer Setup options may vary depending on the hardware configuration.

Table 8-3
Setup Utility

Heading	Option	Description
	DriveLock Security	Allows you to assign or modify a master or user password for MultiBay hard drives. When this feature is enabled, the user is prompted to provide one of the DriveLock passwords during POST. If neither is successfully entered, the hard drive will remain inaccessible until one of the passwords is successfully provided during a subsequent cold-boot sequence. This selection will only appear when at least one MultiBay drive that supports the DriveLock feature is attached to the system. See the *Desktop Management Guide* on the *Documentation CD* for more information.
	Data Execution Prevention	Enable/Disable. Data Execution Prevention Mode help prevent OS security breaches. This selection is in effect only if the processor and operating system being used comprehend and utilize the function.
Security *(continued)*	Master Boot Record Security*	Allows you to enable or disable Master Boot Record (MBR) Security. When enabled, the BIOS rejects all requests to write to the MBR on the current bootable disk. Each time the computer is powered on or rebooted, the BIOS compares the MBR of the bootable disk to the previously saved MBR. If changes are detected, you are given the option of saving the MBR on the current bootable disk, restoring the previously-saved MBR, or disabling MBR security. You must know the setup password if one is set. Disable MBR Security before intentionally changing the formatting or partitioning of the current bootable disk. Several disk utilities (such as FDISK and FORMAT) attempt to update the MBR. If MBR Security is enabled and disk accesses are being serviced by the BIOS, write requests to the MBR are rejected, causing the utilities to report errors. If MBR Security is enabled and disk accesses are being serviced by the operating system, any MBR change will be detected by the BIOS during the next reboot, and an MBR Security warning message will be displayed.
	Save Master Boot Record*	Saves a backup copy of the Master Boot Record of the current bootable disk. Only appears if MBR Security is enabled.

Support for specific Computer Setup options may vary depending on the hardware configuration.

Table 8-3
Setup Utility

Heading	Option	Description
	Restore Master Boot Record*	Restores the backup Master Boot Record to the current bootable disk. Only appears if all of the following conditions are true: MBR Security is enabled. A backup copy of the MBR has been previously saved. The current bootable disk is the same disk from which the backup copy of the MBR was saved. **CAUTION:** Restoring a previously saved MBR after a disk utility or operating system has modified the MBR may cause the data on the disk to become inaccessible. Only restore a previously saved MBR ifyou are confident that the current bootable disk's MBR has been corrupted or infected with a virus.
Power	OS Power Management	• Runtime Power Management - Enable/Disable. Allows certain operating systems to reduce processor voltage and frequency when the current software load does not require the full capabilities of the processor. • Idle Power Savings - Extended/Normal. Allows certain operating systems to decrease the processors power consumption when the processor is idle. • ACPI S3 Support - Enables or disables ACPI S3 support. • ACPI S3 Hard Disk Reset - Enabling this causes the BIOS to ensure hard disks are ready to accept commands after resuming from S3 before returning control to the operating system. • ACPI S3 PS2 Mouse Wakeup - Enables or disables waking from S3 due to PS2 mouse activity.
	Hardware Power Management	SATA power management enables or disables SATA bus and/or device power management.
	Thermal	Fan idle mode - This bar graph controls the minimum permitted fan speed.

Support for specific Computer Setup options may vary depending on the hardware configuration.

Table 8-3
Setup Utility

Heading	Option	Description
Advanced* *For advanced users only	Power-On Options	Allows you to set: • POST mode (QuickBoot, FullBoot, or FullBoot every 1-30 days). • POST messages (enable/disable). • **F9** prompt (enable/disable). Enabling this feature will display the text **F9=Boot Menu** during POST. Disabling this feature prevents the text from being displayed but pressing **F9** will still access the Shortcut Boot (Order) Menu screen. See **Storage > Boot Order** for more information. • **F10** prompt (enable/disable). Enabling this feature will display the text **F10=Setup** during POST. Disabling this feature prevents the text from being displayed but pressing **F10** will still access the Setup screen. • **F12** prompt (enable/disable). Enabling this feature will display the text **F12=Network Service Boot** during POST. Disabling this feature prevents the text from being displayed but pressing **F12** will still force the system to attempt booting from the network. • Option ROM* prompt (enable/disable). Enabling this feature will cause the system to display a message before loading options ROMs. (This feature is supported on select models only.) • Remote wakeup boot source (remote server/local hard drive). • After Power Loss (off/on/previous state): After power loss, if you connect your computer to an electric power strip and would like to turn on power to the computer using the switch on the power strip, set this option to **ON**. ✎ If you turn off power to your computer using the switch on a power strip, you will not be able to use the suspend/sleep feature or the Remote Management features. • POST Delay (in seconds) (enable/disable). Enabling this feature will add a user-specified delay to the POST process. This delay is sometimes needed for hard disks on some PCI cards that spin up very slowly; so slowly that they are not ready to boot by the time POST is finished. The POST delay also gives you more time to press **F10** to enter Computer (F10) Setup. • I/O APIC Mode (enable/disable). Enabling this feature will allow Microsoft Windows Operating Systems to run optimally. This feature must be disabled for certain non-Microsoft Operating Systems to work properly.

✎ Support for specific Computer Setup options may vary depending on the hardware configuration.

Table 8-3
Setup Utility

Heading	Option	Description
Advanced* *(continued)* *For advanced users only	Power-On Options *(continued)*	Allows you to set: (continued) • ACPI/USB Buffers @ Top of Memory (enable/disable). Enabling this feature places USB memory buffers at the top of memory. The advantage is that some amount of memory below 1 MB is freed up for use by option ROMs. The disadvantage is that a popular memory manager, HIMEM.SYS, does not work properly when USB buffers are at top of memory AND the system has 64 MB or less of RAM. • Hyper-threading (enable/disable). • Limit CPUID Maximum Value to 3 - Restricts the number of CPUID functions reported by the microprocessor. Enable this feature if booting to WinNT.
	BIOS Power-On	Allows you to set the computer to turn on automatically at a time you specify.
	Onboard Devices	Allows you to set resources for or disable onboard system devices (diskette controller, serial port, or parallel port).
	PCI Devices	• Lists currently installed PCI devices and their IRQ settings. • Allows you to reconfigure IRQ settings for these devices or to disable them entirely. These settings have no effect under an APIC-based operating system.
	Bus Options*	On select models, allows you to enable or disable: • PCI SERR# Generation. • PCI VGA palette snooping, which sets the VGA palette snooping bit in PCI configuration space; only needed when more than one graphics controller is installed.

Support for specific Computer Setup options may vary depending on the hardware configuration.

Table 8-3
Setup Utility

Heading	Option	Description

Advanced* *(continued)* *For advanced users only	Device options	Allows you to set:
		• Printer mode (bi-directional, EPP & ECP, output only).
		• **Num Lock** state at power-on (off/on).
		• S5 Wake on LAN (enable/disable).
		  • To disable Wake on LAN during the off state (S5), use the arrow (left and right) keys to select the **Advanced** > **Device Options** menu and set the S5 Wake on Lan feature to "Disable." This obtains the lowest power consumption available on the computer during S5. It does not affect the ability of the computer to Wake on LAN from suspend or hibernation, but will prevent it from waking from S5 via the network. It does not affect operation of the network connection while the computer is on.
		  • If a network connection is not required, completely disable the network controller (NIC) by using the arrow (left and right) keys to select the **Security** > **Device Security** menu. Set the Network Controller option to "Device Hidden." This prevents the network controller from being used by the operating system and reduces the power used by the computer in S5.
		• Processor cache (enable/disable).
		• Unique Sleep State Blink Patterns. Allows you to choose an LED blink pattern that uniquely identifies each sleep state.
		• Integrated Video (enable/disable) Allows you to use integrated video and PCI Up Solution video at the same time (available on select models only).
		Inserting a PCI or PCI Express video card automatically disables Integrated Video. When PCI Express video is on, Integrated Video must remain disabled.
		• Monitor Tracking (enable/disable). Allows ROM to save monitor asset information.

		Allows you to set: • NIC PXE Option ROM Download (enable/disable). The BIOS contains an embedded NIC option ROM to allow the unit to boot through the network to a PXE server. This is typically used to download a corporate image to a hard drive. The NIC option ROM takes up memory space below 1MB commonly referred to as DOS Compatibility Hole (DCH) space. This space is limited. This F10 option will allow users to disable the downloading of this embedded NIC option ROM thus giving more DCH space for additional PCI cards which may need option ROM space. The default will be to have the NIC option ROM enabled.
	PCI VGA Configuration	Displayed only if there are multiple PCI video adapters in the system. Allows you to specify which VGA controller will be the "boot" or primary VGA controller.

Support for specific Computer Setup options may vary depending on the hardware configuration.

8.5 Client Management Functions

Table 8-4 provides a partial list of the client management BIOS functions supported by the systems covered in this guide. These functions, designed to support intelligent manageability applications, are Compaq-specific unless otherwise indicated.

Table 8-4.
Client Management Functions (INT15)

AX	Function	Mode
E800h	Get system ID	Real, 16-, & 32-bit Prot.
E813h	Get monitor data	Real, 16-, & 32-bit Prot.
E814h	Get system revision	Real, 16-, & 32-bit Prot.
E816h	Get temperature status	Real, 16-, & 32-bit Prot.
E817h	Get drive attribute	Real
E818h	Get drive off-line test	Real
E819h	Get chassis serial number	Real, 16-, & 32-bit Prot.
E820h [1]	Get system memory map	Real
E81Ah	Write chassis serial number	Real
E81Bh	Get hard drive threshold	Real
E81Eh	Get hard drive ID	Real
E827h	DIMM EEPROM Access	Real, 16-, & 32-bit Prot.

NOTE:
[1] Industry standard function.

All 32-bit protected-mode functions are accessed by using the industry-standard BIOS32 Service Directory. Using the service directory involves three steps:

1. Locating the service directory.
2. Using the service directory to obtain the entry point for the client management functions.
3. Calling the client management service to perform the desired function.

The BIOS32 Service Directory is a 16-byte block that begins on a 16-byte boundary between the physical address range of 0E0000h-0FFFFFh.

The following subsections provide a brief description of key Client Management functions.

8.5.1 System ID and ROM Type

Diagnostic applications can use the INT 15, AX=E800h BIOS function to identify the type of system. This function will return the system ID in the BX register. systems have the following IDs and ROM family types:

Table 8-5
System ID

System (Form Factor)	System ID
USDT	0980h
SFF/ ST:	097Ch
uT:	0984h
CMT:	0968h

NOTE: All systems use BIOS ROM Family 786C1 and PnP ID CPQ0968.

The ROM family and version numbers can be verified with the Setup utility or the Compaq Insight Manager or Diagnostics applications.

8.5.2 Temperature Status

The BIOS includes a function (INT15, AX=E816h) to retrieve the status of a system's interior temperature. This function allows an application to check whether the temperature situation is at a Normal, Caution, or Critical condition.

8.5.3 Drive Fault Prediction

The BIOS directly supports Drive Fault Prediction for IDE (ATA)-type hard drives. This feature is provided through two Client Management BIOS calls. Function INT 15, AX=E817h is used to retrieve a 512-byte block of drive attribute data while the INT 15, AX=E81Bh is used to retrieve the drive's warranty threshold data. If data is returned indicating possible failure then the following message is displayed:

1720-SMART Hard Drive detects imminent failure

8.6 PnP Support

The BIOS includes Plug 'n Play (PnP) support for PnP version 1.0A. Table 8-6 lists the PnP functions supported.

Table 8-6.
PnP BIOS Functions

Function	Register
00h	Get number of system device nodes
01h	Get system device node
02h	Set system device node
03h	Get event
04h	Send message
50h	Get SMBIOS Structure Information
51h	Get Specific SMBIOS Structure

The BIOS call INT 15, AX=E841h, BH=01h can be used by an application to retrieve the default settings of PnP devices for the user. The application should use the following steps for the display function:

1. Call PnP function 01(get System Device Node) for each devnode with bit 1 of the control flag set (get static configuration) and save the results.
2. Call INT 15, AX=E841h, BH=01h.
3. Call PnP “Get Static Configuration” for each devnode and display the defaults.
4. If the user chooses to save the configuration, no further action is required. The system board devices will be configured at the next boot. If the user wants to abandon the changes, then the application must call PnP function 02 (Set System Device Node) for each devnode (with bit 1 of the control flag set for static configuration) with the results from the calls made prior to invoking this function.

8.6.1 SMBIOS

In support of the DMI specification the PnP functions 50h and 51h are used to retrieve the SMBIOS data. Function 50h retrieves the number of structures, size of the largest structure, and SMBIOS version. Function 51h retrieves a specific structure. This system supports SMBIOS version 2.3.1 and the following structure types:

Type	Data
0	BIOS Information
1	System Information
3	System Enclosure or Chassis
4	Processor Information
7	Cache Information
8	Port Connector Information
9	System Slots
13	BIOS Language Information
15	System Event Log Information
16	Physical Memory Array
17	Memory Devices
19	Memory Array Mapped Addresses
20	Memory Device Mapped Addresses
31	Boot Integrity Service Entry Point
32	System Boot Information
128	OEM Defined Structure with Intel Alert-On-LAN (AOL) Information

System information on these systems is handled exclusively through the SMBIOS.

8.7 USB Legacy Support

The BIOS ROM checks the USB port, during POST, for the presence of a USB keyboard. This allows a system with only a USB keyboard to be used during ROM-based setup and also on a system with an OS that does not include a USB driver.

On such a system a keystroke will generate an SMI and the SMI handler will retrieve the data from the device and convert it to PS/2 data. The data will be passed to the keyboard controller and processed as in the PS/2 interface. Changing the delay and/or typematic rate of a USB keyboard though BIOS function INT 16 is not supported.

A

Error Messages and Codes

A.1 Introduction

This appendix lists the error codes and a brief description of the probable cause of the error.

Errors listed in this appendix are applicable only for systems running HP/Compaq BIOS.

Not all errors listed in this appendix may be applicable to a particular system model and/or configuration.

A.2 Beep/Keyboard LED Codes

Beep and LED indictions listed in Table A-1 apply only to HP-branded models.

Table A-1.
Beep/Keyboard LED Codes

Beeps	LED [1]	Probable Cause
1 short, 2 long	NUM lock blinking	Base memory failure.
1 long, 2 short	CAP lock blinking	Video/graphics controller failure.
2 long, 1 short	Scroll lock blinking	System failure (prior to video initialization).
1 long, 3 short	(None)	Boot block executing
None	All three blink in sequence	Keyboard locked in network mode.
None	NUM lock steady on	ROMPAQ diskette not present, bad, or drive not ready.
None	CAP lock steady on	Password prompt.
None	All three blink together	ROM flash failed.
None	All three steady on	Successful ROM flash.

NOTES:

[1] PS/2 keyboard only.

A.3 Power-On Self Test (POST) Messages

Table A-2.
Power-On Self Test (POST) Messages

Error Message	Probable Cause
Invalid Electronic Serial Number	Chassis serial number is corrupt. Use Setup to enter a valid number.
Network Server Mode Active (w/o kybd)	System is in network mode.
101-Option ROM Checksum Error	A device's option ROM has failed/is bad.
110-Out of Memory Space for Option ROMs	Recently added PCI card contains and option ROM too large to download during POST.
102-system Board Failure	Failed ESCD write, A20, timer, or DMA controller.
150-Safe POST Active	An option ROM failed to execute on a previous boot.
162-System Options Not Set	Invalid checksum, RTC lost power, or invalid configuration.
163-Time & Date Not Set	Date and time information in CMOS is not valid.
164-Memory Size Error	Memory has been added or removed.
201-Memory Error	Memory test failed.
213-Incompatible Memory Module	BIOS detected installed DIMM(s) as being not compatible.
214-DIM Configuration Warning	A specific error has occurred in a memory device installed in the identified socket.
216-Memory Size Exceeds Max	Installed memory exceeds the maximum supported by the system.
217-DIMM Configuration Warning	Unbalanced memory configuration.
219-ECC Memory Module Detected ECC Modules not supported on this platform	Recently added memory module(s) support ECC memory error correction.
301-Keyboard Error	Keyboard interface test failed (improper connection or stuck key).
303-Keyboard Controller Error	Keyboard buffer failed empty (8042 failure or stuck key).
304-Keyboard/System Unit Error	Keyboard controller failed self-test.
404-Parallel Port Address Conflict	Current parallel port address is conflicting with another device.
417-Network Interface Card Failure	NIC BIOS could not read Device ID of embedded NIC.
501-Display Adapter Failure	Graphics display controller.
510-Splash Image Corrupt	Corrupted splash screen image. Restore default image w/ROMPAQ.
511-CPU Fan Not Detected	Processor heat sink fan is not connected.

Table A-2. *(Continued)*
Power-On Self Test (POST) Messages

Error Message	Probable Cause
512-Chassis Fan Not Detected	Chassis fan is not connected.
514-CPU or Chassis Fan not detected.	CPU fan is not connected or may have malfunctioned.
601-Diskette Controller Error	Diskette drive removed since previous boot.
605-Diskette Drive Type Error	Mismatch in drive type.
912-Computer Cover Removed Since Last System Start Up	Cover (hood) removal has been detected by the Smart Cover Sensor.
914-Hood Lock Coil is not Connected	Smart Cover Lock mechanism is missing or not connected.
916-Power Button Not Connected	Power button harness has been detached or unseated from the system board.
917-Expansion Riser Not Detected	Expansion (backplane) board not seated properly.
919-Front Panel, MultiPort, and/or MultiBay Risers not Detected	Riser card has been removed or has not been reinstalled properly in the system.
1156-Serial Port A Cable Not Detected	Cable from serial port header to I/O connector is missing or not connected properly.
1157-Front Cables Not Detected	Cable from front panel USB and audio connectors is missing or not connected properly.
1720-SMART Hard Drive Detects Imminent Failure	SMART circuitry on an IDE drive has detected possible equipment failure.
1721-SMART SCSI Hard Drive Detects Imminent Failure	SMART circuitry on a SCSI drive has detected possible equipment failure.
1785-MultiBay incorrectly installed	**For MultiBay option or non-USDT systems**: Multibay option ribbon cables not seated or improperly attached. or MultiBay device not properly seated. or MultiBay diskette present **For integrated MultiBay/ USDT systems**: MultiBay device not properly seated. or MultiBay riser not properly seated.
1794–Inaccessible device attached to SATA 1 *(for systems with 2 SATA ports)*	A device is attached to SATA 1. Any device attached to this connector will be inaccessible while "SATA Emulation" is set to "Combined IDE Controller" in Computer Setup.

Table A-2. *(Continued)*
Power-On Self Test (POST) Messages

Error Message	Probable Cause
1794-Inaccessible devices attached to SATA 1 and/or SATA 3 *(for systems with 4 SATA ports)*	A device is attached to SATA 1 and/or SATA 3. Devices attached to these connectors will be inaccessible while "SATA Emulation" is set to "Combined IDE Controller" in Computer Setup
1796-SATA Cabling Error	One or more SATA devices are improperly attached. For optimal performance, the SATA 0 and SATA 1 connectors must be used before SATA 2 and SATA 3.
1801-Microcode Patch Error	A processor is installed for which the BIOS ROM has no patch. Check for ROM update.
1998-Master Boot Record Backup Has Been Lost	Backup copy of the hard drive master boot record is corrupted. Use Setup to restore the backup from the hard drive.
1999-Master Boot Record Has Changed. Press Any Key To Enter Setup to Restore the MBR.	If Master Boot Record Security is enabled, this message indicates that the MBR has changed since the backup was made.
2000-Master boot Record hard drive has changed	The hard drive has been changed. Use Setup to create a backup of the new hard drive.
Invalid Electronic Serial Number	Electronic serial number has become corrupted.
Network Server Mode Active and No Keyboard Attached	Keyboard failure while Network Server Mode enabled.
Parity Check 2	Keyboard failure while Network Server Mode enabled.

A.4 System Error Messages (1xx-xx)

Table A-3.
System Error Messages

Message	Probable Cause	Message	Probable Cause
101	Option ROM error	109-02	CMOS clock rollover test failed
102	System board failure [1]	109-03	CMOS not properly initialized (clk test)
103	System board failure	110-01	Programmable timer load data test failed
104-01	Master int. cntlr. test fialed	110-02	Programmable timer dynamic test failed
104-02	Slave int. cntlr. test failed	110-03	Program timer 2 load data test failed
104-03	Int. cntlr. SW RTC inoperative	111-01	Refresh detect test failed
105-01	Port 61 bit <6> not at zero	112-01	Speed test Slow mode out of range
105-02	Port 61 bit <5> not at zero	112-02	Speed test Mixed mode out of range
105-03	Port 61 bit <3> not at zero	112-03	Speed test Fast mode out of range
105-04	Port 61 bit <1> not at zero	112-04	Speed test unable to enter Slow mode
105-05	Port 61 bit <0> not at zero	112-05	Speed test unable to enter Mixed mode
105-06	Port 61 bit <5> not at one	112-06	Speed test unable to enter Fast mode
105-07	Port 61 bit <3> not at one	112-07	Speed test system error
105-08	Port 61 bit <1> not at one	112-08	Unable to enter Auto mode in speed test
105-09	Port 61 bit <0> not at one	112-09	Unable to enter High mode in speed test
105-10	Port 61 I/O test failed	112-10	Speed test High mode out of range
105-11	Port 61 bit <7> not at zero	112-11	Speed test Auto mode out of range
105-12	Port 61 bit <2> not at zero	112-12	Speed test variable speed mode inop.
105-13	No int. generated by failsafe timer	113-01	Protected mode test failed
105-14	NMI not triggered by failsafe timer	114-01	Speaker test failed
106-01	Keyboard controller test failed	116-xx	Way 0 read/write test failed
107-01	CMOS RAM test failed	162-xx	Sys. options failed (mismatch in drive type)
108-02	CMOS interrupt test failed	163-xx	Time and date not set
108-03	CMOS not properly initialized (int.test)	164-xx	Memory size
109-01	CMOS clock load data test failed	199-00	Installed devices test failed

NOTES:
[1] 102 message code may be caused by one of a variety of processor-related problems that may be solved by replacing the processor, although system board replacement may be needed.

A.5 Memory Error Messages (2xx-xx)

Table A-4.
Memory Error Messages

Message	Probable Cause
200-04	Real memory size changed
200-05	Extended memory size changed
200-06	Invalid memory configuration
200-07	Extended memory size changed
200-08	CLIM memory size changed
201-01	Memory machine ID test failed
202-01	Memory system ROM checksum failed
202-02	Failed RAM/ROM map test
202-03	Failed RAM/ROM protect test
203-01	Memory read/write test failed
203-02	Error while saving block in read/write test
203-03	Error while restoring block in read/write test
204-01	Memory address test failed
204-02	Error while saving block in address test
204-03	Error while restoring block in address test
204-04	A20 address test failed
204-05	Page hit address test failed
205-01	Walking I/O test failed
205-02	Error while saving block in walking I/O test
205-03	Error while restoring block in walking I/O test
206-xx	Increment pattern test failed
207-xx	ECC failure
210-01	Memory increment pattern test
210-02	Error while saving memory during increment pattern test
210-03	Error while restoring memory during increment pattern test
211-01	Memory random pattern test

Table A-4. *(Continued)*
Memory Error Messages

Message	Probable Cause
211-02	Error while saving memory during random memory pattern test
211-03	Error while restoring memory during random memory pattern test
213-xx	Incompatible DIMM in slot x
214-xx	Noise test failed
215-xx	Random address test

A.6 Keyboard Error Messages (30x-xx)

Table A-5.
Keyboard Error Messages

Message	Probable Cause	Message	Probable Cause
300-xx	Failed ID test	303-05	LED test, LED command test failed
301-01	Kybd short test, 8042 self-test failed	303-06	LED test, LED command test failed
301-02	Kybd short test, interface test failed	303-07	LED test, LED command test failed
301-03	Kybd short test, echo test failed	303-08	LED test, command byte restore test failed
301-04	Kybd short test, kybd reset failed	303-09	LED test, LEDs failed to light
301-05	Kybd short test, kybd reset failed	304-01	Keyboard repeat key test failed
302-xx	Failed individual key test	304-02	Unable to enter mode 3
302-01	Kybd long test failed	304-03	Incorrect scan code from keyboard
303-01	LED test, 8042 self-test failed	304-04	No Make code observed
303-02	LED test, reset test failed	304-05	Cannot /disable repeat key feature
303-03	LED test, reset failed	304-06	Unable to return to Normal mode
303-04	LED test, LED command test failed	--	--

A.7 Printer Error Messages (4xx-xx)

Table A-6
Printer Error Messages

Message	Probable Cause	Message	Probable Cause
401-01	Printer failed or not connected	402-11	Interrupt test, data/cntrl. reg. failed
402-01	Printer data register failed	402-12	Interrupt test and loopback test failed
402-02	Printer control register failed	402-13	Int. test, LpBk. test., and data register failed
402-03	Data and control registers failed	402-14	Int. test, LpBk. test., and cntrl. register failed
402-04	Loopback test failed	402-15	Int. test, LpBk. test., and data/cntrl. reg. failed
402-05	Loopback test and data reg. failed	402-16	Unexpected interrupt received
402-06	Loopback test and cntrl. reg. failed	402-01	Printer pattern test failed
402-07	Loopback tst, data/cntrl. reg. failed	403-xx	Printer pattern test failed
402-08	Interrupt test failed	404-xx	Parallel port address conflict
402-09	Interrupt test and data reg. failed	498-00	Printer failed or not connected
402-10	Interrupt test and control reg. failed	--	--

A.8 Video (Graphics) Error Messages (5xx-xx)

Table A-7.
Video (Graphics) Error Messages

Message	Probable Cause	Message	Probable Cause
501-01	Video controller test failed	508-01	320x200 mode, color set 0 test failed
502-01	Video memory test failed	509-01	320x200 mode, color set 1 test failed
503-01	Video attribute test failed	510-01	640x200 mode test failed
504-01	Video character set test failed	511-01	Screen memory page test failed
505-01	80x25 mode, 9x14 cell test failed	512-01	Gray scale test failed
506-01	80x25 mode, 8x8 cell test failed	514-01	White screen test failed
507-01	40x25 mode test failed	516-01	Noise pattern test failed

See Table A-14 for additional video (graphics) messages.

A.9 Diskette Drive Error Messages (6xx-xx)

Table A-8.
Diskette Drive Error Messages

Message	Probable Cause	Message	Probable Cause
6xx-01	Exceeded maximum soft error limit	6xx-20	Failed to get drive type
6xx-02	Exceeded maximum hard error limit	6xx-21	Failed to get change line status
6xx-03	Previously exceeded max soft limit	6xx-22	Failed to clear change line status
6xx-04	Previously exceeded max hard limit	6xx-23	Failed to set drive type in ID media
6xx-05	Failed to reset controller	6xx-24	Failed to read diskette media
6xx-06	Fatal error while reading	6xx-25	Failed to verify diskette media
6xx-07	Fatal error while writing	6xx-26	Failed to read media in speed test
6xx-08	Failed compare of R/W buffers	6xx-27	Failed speed limits
6xx-09	Failed to format a tract	6xx-28	Failed write-protect test
6xx-10	Failed sector wrap test	--	--

600-xx = Diskette drive ID test
601-xx = Diskette drive format
602-xx = Diskette read test
603-xx = Diskette drive R/W compare test
604-xx = Diskette drive random seek test
605-xx = Diskette drive ID media
606-xx = Diskette drive speed test
607-xx = Diskette drive wrap test
608-xx = Diskette drive write-protect test
609-xx = Diskette drive reset controller test
610-xx = Diskette drive change line test
611-xx = Pri. diskette drive port addr. conflict
612-xx = Sec. diskette drive port addr. conflict
694-00 = Pin 34 not cut on 360-KB drive
697-00 = Diskette type error
698-00 = Drive speed not within limits
699-00 = Drive/media ID error (run Setup)

A.10 Serial Interface Error Messages (11xx-xx)

Table A-9.
Serial Interface Error Messages

Message	Probable Cause	Message	Probable Cause
1101-01	UART DLAB bit failure	1101-13	UART cntrl. signal interrupt failure
1101-02	Line input or UART fault	1101-14	DRVR/RCVR data failure
1101-03	Address line fault	1109-01	Clock register initialization failure
1101-04	Data line fault	1109-02	Clock register rollover failure
1101-05	UART cntrl. signal failure	1109-03	Clock reset failure
1101-06	UART THRE bit failure	1109-04	Input line or clock failure
1101-07	UART Data RDY bit failure	1109-05	Address line fault
1101-08	UART TX/RX buffer failure	1109-06	Data line fault
1101-09	Interrupt circuit failure	1150-xx	Comm port setup error (run Setup)
1101-10	COM1 set to invalid INT	1151-xx	COM1 address conflict
1101-11	COM2 set to invalid INT	1152-xx	COM2 address conflict
1101-12	DRVR/RCVR cntrl. signal failure	1155-xx	COM port address conflict

A.11 Modem Communications Error Messages (12xx-xx)

Table A-10.
Modem Communications Error Messages

Message	Probable Cause	Message	Probable Cause
1201-XX	Modem internal loopback test	1204-03	Data block retry limit reached [4]
1201-01	UART DLAB bit failure	1204-04	RX exceeded carrier lost limit
1201-02	Line input or UART failure	1204-05	TX exceeded carrier lost limit
1201-03	Address line failure	1204-06	Time-out waiting for dial tone
1201-04	Data line fault	1204-07	Dial number string too long
1201-05	UART control signal failure	1204-08	Modem time-out waiting for remote response
1201-06	UART THRE bit failure	1204-09	Modem exceeded maximum redial limit
1201-07	UART DATA READY bit failure	1204-10	Line quality prevented remote response
1201-08	UART TX/RX buffer failure	1204-11	Modem time-out waiting for remote connection
1201-09	Interrupt circuit failure	1205-XX	Modem auto answer test
1201-10	COM1 set to invalid inturrupt	1205-01	Time-out waiting for SYNC [5]
1201-11	COM2 set to invalid	1205-02	Time-out waiting for response [5]
1201-12	DRVR/RCVR control signal failure	1205-03	Data block retry limit reached [5]
1201-13	UART control signal interrupt failure	1205-04	RX exceeded carrier lost limit
1201-14	DRVR/RCVR data failure	1205-05	TX exceeded carrier lost limit
1201-15	Modem detection failure	1205-06	Time-out waiting for dial tone
1201-16	Modem ROM, checksum failure	1205-07	Dial number string too long
1201-17	Tone detect failure	1205-08	Modem time-out waiting for remote response
1202-XX	Modem internal test	1205-09	Modem exceeded maximum redial limit
1202-01	Time-out waiting for SYNC [1]	1205-10	Line quality prevented remote response
1202-02	Time-out waiting for response [1]	1205-11	Modem time-out waiting for remote connection
1202-03	Data block retry limit reached [1]	1206-XX	Dial multi-frequency tone test
1202-11	Time-out waiting for SYNC [2]	1206-17	Tone detection failure
1202-12	Time-out waiting for response [2]	1210-XX	Modem direct connect test

Table A-10. *(Continued)*
Modem Communications Error Messages

Message	Probable Cause	Message	Probable Cause
1202-13	Data block retry limit reached [2]	1210-01	Time-out waiting for SYNC [6]
1202-21	Time-out waiting for SYNC [3]	1210-02	Time-out waiting for response [6]
1202-22	Time-out waiting for response [3]	1210-03	Data block retry limit reached [6]
1202-23	Data block retry limit reached [3]	1210-04	RX exceeded carrier lost limit
1203-XX	Modem external termination test	1210-05	TX exceeded carrier lost limit
1203-01	Modem external TIP/RING failure	1210-06	Time-out waiting for dial tone
1203-02	Modem external data TIP/RING fail	1210-07	Dial number string too long
1203-03	Modem line termination failure	1210-08	Modem time-out waiting for remote response
1204-XX	Modem auto originate test	1210-09	Modem exceeded maximum redial limit
1204-01	Time-out waiting for SYNC [4]	1210-10	Line quality prevented remote response
1204-02	Time-out waiting for response [4]	1210-11	Modem time-out waiting for remote connection

NOTES:

[1] Local loopback mode
[2] Analog loopback originate mode
[3] Analog loopback answer mode
[4] Modem auto originate test
[5] Modem auto answer test
[6] Modem direct connect test

A.12 System Status Error Messages (16xx-xx)

Table A-11
System Status Error Messages

Message	Probable Cause
1601-xx	Temperature violation
1611-xx	Fan failure

A.13 Hard Drive Error Messages (17xx-xx)

Table A-12
Hard Drive Error Messages

Message	Probable Cause	Message	Probable Cause
17xx-01	Exceeded max. soft error limit	17xx-51	Failed I/O read test
17xx-02	Exceeded max. Hard error limit	17xx-52	Failed file I/O compare test
17xx-03	Previously exceeded max. soft error limit	17xx-53	Failed drive/head register test
17xx-04	Previously exceeded max.hard error limit	17xx-54	Failed digital input register test
17xx-05	Failed to reset controller	17xx-55	Cylinder 1 error
17xx-06	Fatal error while reading	17xx-56	Failed controller RAM diagnostics
17xx-07	Fatal error while writing	17xx-57	Failed controller-to-drive diagnostics
17xx-08	Failed compare of R/W buffers	17xx-58	Failed to write sector buffer
17xx-09	Failed to format a track	17xx-59	Failed to read sector buffer
17xx-10	Failed diskette sector wrap during read	17xx-60	Failed uncorrectable ECC error
17xx-19	Cntlr. failed to deallocate bad sectors	17xx-62	Failed correctable ECC error
17xx-40	Cylinder 0 error	17xx-63	Failed soft error rate
17xx-41	Drive not ready	17xx-65	Exceeded max. bad sectors per track
17xx-42	Failed to recalibrate drive	17xx-66	Failed to initialize drive parameter
17xx-43	Failed to format a bad track	17xx-67	Failed to write long
17xx-44	Failed controller diagnostics	17xx-68	Failed to read long
17xx-45	Failed to get drive parameters from ROM	17xx-69	Failed to read drive size
17xx-46	Invalid drive parameters from ROM	17xx-70	Failed translate mode
17xx-47	Failed to park heads	17xx-71	Failed non-translate mode
17xx-48	Failed to move hard drive table to RAM	17xx-72	Bad track limit exceeded
17xx-49	Failed to read media in file write test	17xx-73	Previously exceeded bad track limit
17xx-50	Failed I/O write test	--	--

NOTE:

xx = 00, Hard drive ID test
xx = 01, Hard drive format test
xx = 02, Hard drive read test
xx = 03, Hard drive read/write compare test
xx = 04, Hard drive random seek test
xx = 05, Hard drive controller test
xx = 06, Hard drive ready test
xx = 07, Hard drive recalibrate test
xx = 08, Hard drive format bad track test
xx = 09, Hard drive reset controller test
xx = 10, Hard drive park head test
xx = 14, Hard drive file write test
xx = 15, Hard drive head select test
xx = 16, Hard drive conditional format test
xx = 17, Hard drive ECC test
xx = 19, Hard drive power mode test
xx = 20, SMART drive detects imminent failure
xx = 21, SCSI hard drive imminent failure
xx = 24, Net work preparation test
xx = 36, Drive monitoring test
xx = 71, Pri. IDE controller address conflict
xx = 72, Sec. IDE controller address conflict
xx = 80, Disk 0 failure
xx = 81, Disk 1 failure
xx = 82, Pri. IDE controller failure
xx = 90, Disk 0 failure
xx = 91, Disk 1 failure
xx = 92, Se. controller failure
xx = 93, Sec. Controller or disk failure
xx = 99, Invalid hard drive type

A.14 Hard Drive Error Messages (19xx-xx)

Table A-13
Hard Drive Error Messages

Message	Probable Cause	Message	Probable Cause
19xx-01	Drive not installed	19xx-21	Got servo pulses second time but not first
19xx-02	Cartridge not installed	19xx-22	Never got to EOT after servo check
19xx-03	Tape motion error	19xx-23	Change line unset
19xx-04	Drive busy erro	19xx-24	Write-protect error
19xx-05	Track seek error	19xx-25	Unable to erase cartridge
19xx-06	Tape write-protect error	19xx-26	Cannot identify drive
19xx-07	Tape already Servo Written	19xx-27	Drive not compatible with controller
19xx-08	Unable to Servo Write	19xx-28	Format gap error
19xx-09	Unable to format	19xx-30	Exception bit not set
19xx-10	Format mode error	19xx-31	Unexpected drive status
19xx-11	Drive recalibration error	19xx-32	Device fault
19xx-12	Tape not Servo Written	19xx-33	Illegal command
19xx-13	Tape not formatted	19xx-34	No data detected
19xx-14	Drive time-out error	19xx-35	Power-on reset occurred
19xx-15	Sensor error flag	19xx-36	Failed to set FLEX format mode
19xx-16	Block locate (block ID) error	19xx-37	Failed to reset FLEX format mode
19xx-17	Soft error limit exceeded	19xx-38	Data mismatch on directory track
19xx-18	Hard error limit exceeded	19xx-39	Data mismatch on track 0
19xx-19	Write (probably ID) error	19xx-40	Failed self-test
19xx-20	NEC fatal error	19xx-91	Power lost during test

1900-xx = Tape ID test failed
1901-xx = Tape servo write failed
1902-xx = Tape format failed
1903-xx = Tape drive sensor test failed
1904-xx = Tape BOT/EOT test failed
1905-xx = Tape read test failed
1906-xx = Tape R/W compare test failed
1907-xx = Tape write-protect failed

A.15 Video (Graphics) Error Messages (24xx-xx)

Table A-14
Video (Graphics) Error Messages

Message	Probable Cause	Message	Probable Cause
2402-01	Video memory test failed	2418-02	EGA shadow RAM test failed
2403-01	Video attribute test failed	2419-01	EGA ROM checksum test failed
2404-01	Video character set test failed	2420-01	EGA attribute test failed
2405-01	80x25 mode, 9x14 cell test failed	2421-01	640x200 mode test failed
2406-01	80x25 mode, 8x8 cell test failed	2422-01	640x350 16-color set test failed
2407-01	40x25 mode test failed	2423-01	640x350 64-color set test failed
2408-01	320x200 mode color set 0 test failed	2424-01	EGA Mono. text mode test failed
2409-01	320x200 mode color set 1 test failed	2425-01	EGA Mono. graphics mode test failed
2410-01	640x200 mode test failed	2431-01	640x480 graphics mode test failed
2411-01	Screen memory page test failed	2432-01	320x200 256-color set test failed
2412-01	Gray scale test failed	2448-01	Advanced VGA controller test failed
2414-01	White screen test failed	2451-01	132-column AVGA test failed
2416-01	Noise pattern test failed	2456-01	AVGA 256-color test failed
2417-01	Lightpen text test failed, no response	2458-xx	AVGA BitBLT test failed
2417-02	Lightpen text test failed, invalid response	2468-xx	AVGA DAC test failed
2417-03	Lightpen graphics test failed, no resp.	2477-xx	AVGA data path test failed
2417-04	Lightpen graphics tst failed, invalid resp.	2478-xx	AVGA BitBLT test failed
2418-01	EGA memory test failed	2480-xx	AVGA linedraw test failed

A.16 Audio Error Messages (3206-xx)

Table A-15
Audio Error Messages

Message	Probable Cause
3206-xx	Audio subsystem internal error

A.17 DVD/CD-ROM Error Messages (33xx-xx)

Table A-16
DVD/CD-ROM Error Messages

Message	Probable Cause
3301-xx	Drive test failed
3305-xx	Seek test failed

A.18 Network Interface Error Messages (60xx-xx)

Table A-17
Network Interface Error Messages

Message	Probable Cause	Message	Probable Cause
6000-xx	Pointing device interface error	6054-xx	Token ring configuration test failed
6014-xx	Ethernet configuration test failed	6056-xx	Token ring reset test failed
6016-xx	Ethernet reset test failed	6068-xx	Token ring int. loopback test failed
6028-xx	Ethernet int. loopback test failed	6069-xx	Token ring ext. loopback test failed
6029-xx	Ethernet ext. loopback test failed	6089-xx	Token ring open

A.19 SCSI Interface Error Messages (65xx-xx, 66xx-xx, 67xx-xx)

Table A-18
SCSI Interface Error Messages

Message	Probable Cause	Message	Probable Cause
6nyy-02	Drive not installed	6nyy-33	Illegal controller command
6nyy-03	Media not installed	6nyy-34	Invalid SCSI bus phase
6nyy-05	Seek failure	6nyy-35	Invalid SCSI bus phase
6nyy-06	Drive timed out	6nyy-36	Invalid SCSI bus phase
6nyy-07	Drive busy	6nyy-39	Error status from drive
6nyy-08	Drive already reserved	6nyy-40	Drive timed out
6nyy-09	Reserved	6nyy-41	SSI bus stayed busy
6nyy-10	Reserved	6nyy-42	ACK/REQ lines bad
6nyy-11	Media soft error	6nyy-43	ACK did not deassert
6nyy-12	Drive not ready	6nyy-44	Parity error
6nyy-13	Media error	6nyy-50	Data pins bad
6nyy-14	Drive hardware error	6nyy-51	Data line 7 bad
6nyy-15	Illegal drive command	6nyy-52	MSG, C/D, or I/O lines bad
6nyy-16	Media was changed	6nyy-53	BSY never went busy
6nyy-17	Tape write-protected	6nyy-54	BSY stayed busy
6nyy-18	No data detected	6nyy-60	Controller CONFIG-1 register fault
6nyy-21	Drive command aborted	6nyy-61	Controller CONFIG-2 register fault
6nyy-24	Media hard error	6nyy-65	Media not unloaded
6nyy-25	Reserved	6nyy-90	Fan failure
6nyy-30	Controller timed out	6nyy-91	Over temperature condition
6nyy-31	Unrecoverable error	6nyy-92	Side panel not installed
6nyy-32	Controller/drive not connected	6nyy-99	Autoloader reported tape not loaded properly

n = 5, Hard drive
= 6, CD-ROM drive
= 7, Tape drive

yy = 00, ID
= 03, Power check
= 05, Read
= 06, SA/Media
= 08, Controller
= 23, Random read
= 28, Media load/unload

A.20 Pointing Device Interface Error Messages (8601-xx)

Table A-19
Pointing Device Interface Error Messages

Message	Probable Cause	Message	Probable Cause
8601-01	Mouse ID fails	8601-07	Right block not selected
8601-02	Left mouse button is inoperative	8601-08	Timeout occurred
8601-03	Left mouse button is stuck closed	8601-09	Mouse loopback test failed
8601-04	Right mouse button is inoperative	8601-10	Pointing device is inoperative
8601-05	Right mouse button is stuck closed	8602-xx	I/F test failed
8601-06	Left block not selected	--	--

B

ASCII Character Set

B.1 Introduction

This appendix lists, in Table B-1, the 256-character ASCII code set including the decimal and hexadecimal values. All ASCII symbols may be called while in DOS or using standard text-mode editors by using the combination keystroke of holding the Alt key and using the Numeric Keypad to enter the decimal value of the symbol. The extended ASCII characters (decimals 128-255) can only be called using the Alt + Numeric Keypad keys.

Regarding keystrokes, refer to notes at the end of the table. Applications may interpret multiple keystroke accesses differently or ignore them completely.

Table B-1.
ASCII Character Set

Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol
0	00	Blank	32	20	Space	64	40	@	96	60	‘
1	01		33	21	!	65	41	A	97	61	a
2	02		34	22	“	66	42	B	98	62	b
3	03	©	35	23	#	67	43	C	99	63	c
4	04	®	36	24	$	68	44	D	100	64	d
5	05	ß	37	25	%	69	45	E	101	65	e
6	06	™	38	26	&	70	46	F	102	66	f
7	07	I	39	27	‘	71	47	G	103	67	g
8	08	m	40	28	(	72	48	H	104	68	h
9	09		41	29	)	73	49	I	105	69	I
10	0A		42	2A	*	74	4A	J	106	6A	j
11	0B		43	2B	+	75	4B	K	107	6B	k
12	0C		44	2C	`	76	4C	L	108	6C	l
13	0D		45	2D	-	77	4D	M	109	6D	m
14	0E		46	2E	.	78	4E	N	110	6E	n
15	0F		47	2F	/	79	4F	O	111	6F	o
16	10	4	48	30	0	80	50	P	112	70	p
17	11	3	49	31	1	81	51	Q	113	71	q

Table B-1. *(Continued)*
ASCII Character Set

Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol
18	12	×	50	32	2	82	52	R	114	72	r
19	13	!!	51	33	3	83	53	S	115	73	s
20	14	¶	52	34	4	84	54	T	116	74	t
21	15	§	53	35	5	85	55	U	117	75	u
22	16	0	54	36	6	86	56	V	118	76	v
23	17	×	55	37	7	87	57	W	119	77	w
24	18	¦	56	38	8	88	58	X	120	78	x
25	19	Ø	57	39	9	89	59	Y	121	79	y
26	1A	Æ	58	3A	:	90	5A	Z	122	7A	z
27	1B	¨	59	3B	;	91	5B	[	123	7B	{
28	1C		60	3C	<	92	5C	\	124	7C	|
29	1D	´	61	3D	=	93	5D	]	125	7D	}
30	1E	s	62	3E	>	94	5E	^	126	7E	~
31	1F	t	63	3F	?	95	5F	_	127	7F	[1]
128	80	Ç	160	A0	á	192	C0		224	E0	
129	81	ü	161	A1	í	193	C1		225	E1	ß
130	82	é	162	A2	ó	194	C2		226	E2	
131	83	â	163	A3	ú	195	C3		227	E3	
132	84	ä	164	A4	ñ	196	C4		228	E4	
133	85	à	165	A5	Ñ	197	C5		229	E5	
134	86	å	166	A6	ª	198	C6		230	E6	µ
135	87	ç	167	A7	º	199	C7		231	E7	
136	88	ê	168	A8	¿	200	C8		232	E8	
137	89	ë	169	A9		201	C9		233	E9	
138	8A	è	170	AA	¬	202	CA		234	EA	
139	8B	ï	171	AB	½	203	CB		235	EB	
140	8C	î	172	AC	¼	204	CC		236	EC	
141	8D	ì	173	AD	¡	205	CD		237	ED	
142	8E	Ä	174	AE	«	206	CE		238	EE	
143	8F	Å	175	AF	»	207	CF		239	EF	
144	90	É	176	B0		208	D0		240	F0	

Table B-1. *(Continued)*
ASCII Character Set

Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol	Dec	Hex	Symbol
145	91	æ	177	B1		209	D1		241	F1	±
146	92	Æ	178	B2		210	D2		242	F2	
147	93	ô	179	B3		211	D3		243	F3	
148	94	ö	180	B4		212	D4		244	F4	
149	95	ò	181	B5		213	D5		245	F5	
150	96	û	182	B6		214	D6		246	F6	÷
151	97	ù	183	B7		215	D7		247	F7	
152	98	ÿ	184	B8		216	D8		248	F8	°
153	99	Ö	185	B9		217	D9		249	F9	·
154	9A	Ü	186	BA		218	DA		250	FA	·
155	9B	¢	187	BB		219	DB		251	FB	
156	9C	£	188	BC		220	DC		252	FC	
157	9D	¥	189	BD		221	DD		253	FD	²
158	9E		190	BE		222	DE		254	FE	
159	9F	ƒ	191	BF		223	DF		255	FF	Blank

NOTES:

[1] Symbol not displayed.

Keystroke Guide:

Dec #	Keystroke(s)
0	Ctrl 2
1-26	Ctrl A thru Z respectively
27	Ctrl [
28	Ctrl
29	Ctrl]
30	Ctrl 6
31	Ctrl -
32	Space Bar
33-43	Shift and key w/corresponding symbol
44-47	Key w/corresponding symbol
48-57	Key w/corresponding symbol, numerical keypad w/Num Lock active
58	Shift and key w/corresponding symbol
59	Key w/corresponding symbol
60	Shift and key w/corresponding symbol
61	Key w/corresponding symbol
62-64	Shift and key w/corresponding symbol
65-90	Shift and key w/corresponding symbol or key w/corresponding symbol and Caps Lock active
91-93	Key w/corresponding symbol
94, 95	Shift and key w/corresponding symbol
96	Key w/corresponding symbol
97-126	Key w/corresponding symbol or Shift and key w/corresponding symbol and Caps Lock active
127	Ctrl -
128-255	Alt and decimal digit(s) of desired character

C

Keyboard

C.1 Introduction

This appendix describes the HP keyboard that is included as standard with the system unit. The keyboard complies with the industry-standard classification of an “enhanced keyboard” and includes a separate cursor control key cluster, twelve “function” keys, and enhanced programmability for additional functions.

This appendix covers the following keyboard types:

- Standard enhanced keyboard.
- Space-Saver Windows-version keyboard featuring additional keys for specific support of the Windows operating system.
- **Easy Access keyboard with additional buttons for internet accessibility functions.**

Only one type of keyboard is supplied with each system. Other types may be available as an option.

This appendix discusses only the keyboard unit. The keyboard interface is a function of the system unit and is discussed in Chapter 5, Input/Output Interfaces.

C.2 Keystroke Processing

A functional block diagram of the keystroke processing elements is shown in Figure C-1. Power (+5 VDC) is obtained from the system through the PS/2-type interface. The keyboard uses a Z86C14 (or equivalent) microprocessor. The Z86C14 scans the key matrix drivers every 10 ms for pressed keys while at the same time monitoring communications with the keyboard interface of the system unit. When a key is pressed, a Make code is generated. A Break code is generated when the key is released. The Make and Break codes are collectively referred to as scan codes. All keys generate Make and Break codes with the exception of the Pause key, which generates a Make code only.

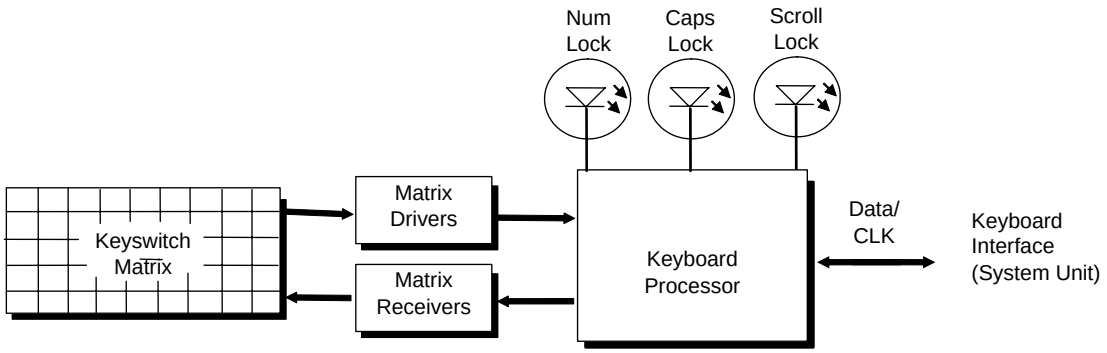


Figure C-1. Keystroke Processing Elements, Block Diagram

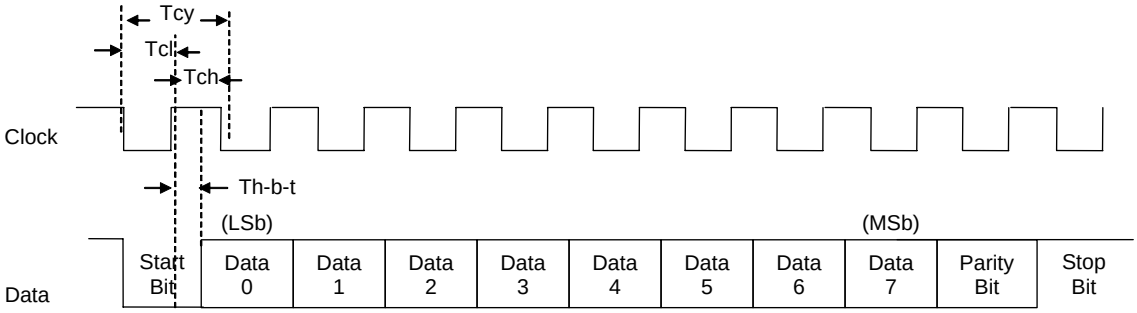
When the system is turned on, the keyboard processor generates a Power-On Reset (POR) signal after a period of 150 ms to 2 seconds. The keyboard undergoes a Basic Assurance Test (BAT) that checks for shorted keys and basic operation of the keyboard processor. The BAT takes from 300 to 500 ms to complete.

If the keyboard fails the BAT, an error code is sent to the CPU and the keyboard is disabled until an input command is received. After successful completion of the POR and BAT, a completion code (AAh) is sent to the CPU and the scanning process begins.

The keyboard processor includes a 16-byte FIFO buffer for holding scan codes until the system is ready to receive them. Response and typematic codes are not buffered. If the buffer is full (16 bytes held) a 17th byte of a successive scan code results in an overrun condition and the overrun code replaces the scan code byte and any additional scan code data (and the respective key strokes) are lost. Multi-byte sequences must fit entirely into the buffer before the respective keystroke can be registered.

C.2.1 PS/2-Type Keyboard Transmissions

The PS/2-type keyboard sends two main types of data to the system; commands (or responses to system commands) and keystroke scan codes. Before the keyboard sends data to the system (specifically, to the 8042-type logic within the system), the keyboard verifies the clock and data lines to the system. If the clock signal is low (0), the keyboard recognizes the inhibited state and loads the data into a buffer. Once the inhibited state is removed, the data is sent to the system. Keyboard-to-system transfers (in the default mode) consist of 11 bits as shown in Figure C-2.



Parameter	Minimum	Nominal	Maximum
Tcy (clock cycle)	60 us	--	80 us
Tcl (clock low)	30 us	41 us	50 us
Tch (clock high)	30 us	--	40 us
Th-b-t (high-before-transmit)	--	20 us	--

Figure C-2. PS/2 Keyboard-To-System Transmission, Timing Diagram

The system can halt keyboard transmission by setting the clock signal low. The keyboard checks the clock line every 60 µs to verify the state of the signal. If a low is detected, the keyboard will finish the current transmission if the rising edge of the clock pulse for the parity bit has not occurred. The system uses the same timing relationships during reads (typically with slightly reduced time periods).

The enhanced keyboard has three operating modes:

- Mode 1—PC-XT compatible
- Mode 2—PC-AT compatible (default)
- Mode 3—Select mode (keys are programmable as to make-only, break-only, typematic)

Modes can be selected by the user or set by the system. Mode 2 is the default mode. Each mode produces a different set of scan codes. When a key is pressed, the keyboard processor sends that key's make code to the 8042 logic of the system unit. The When the key is released, a release code is transmitted as well (except for the Pause key, which produces only a make code). The 8042-type logic of the system unit responds to scan code reception by asserting IRQ1, which is processed by the interrupt logic and serviced by the CPU with an interrupt service routine. The service routine takes the appropriate action based on which key was pressed.

C.2.2 USB-Type Keyboard Transmissions

The USB-type keyboard sends essentially the same information to the system that the PS/2 keyboard does except that the data receives additional NRZI encoding and formatting (prior to leaving the keyboard) to comply with the USB I/F specification (discussed in chapter 5 of this guide).

Packets received at the system's USB I/F and decoded as originating from the keyboard result in an SMI being generated. An SMI handler routine is invoked that decodes the data and transfers the information to the 8042 keyboard controller where normal (legacy) keyboard processing takes place.

C.2.3 Keyboard Layouts

Figures C-3 through C-8 show the key layouts for keyboards shipped with HPsystems. Actual styling details including location of the HP logo as well as the numbers lock, caps lock, and scroll lock LEDs may vary.

C.2.3.1 Standard Enhanced Keyboards

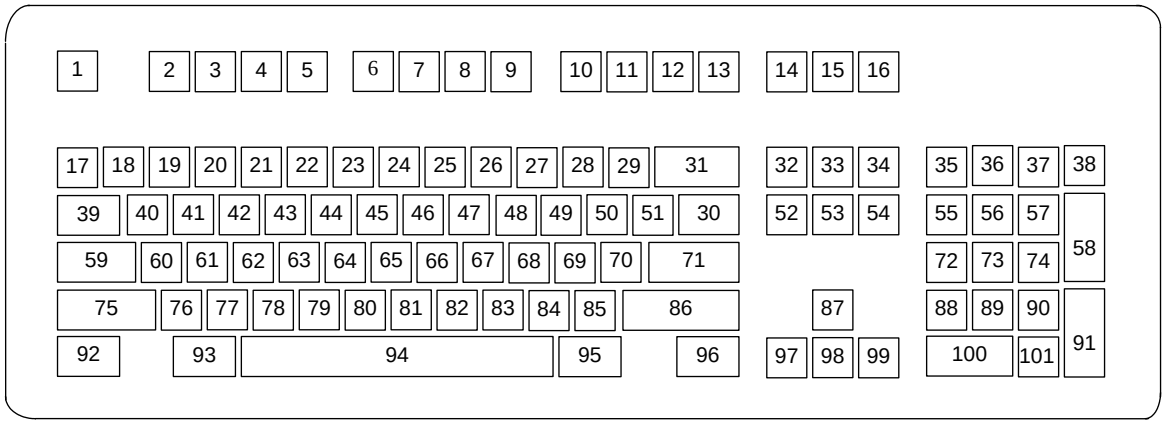


Figure C-3. U.S. English (101-Key) Keyboard Key Positions

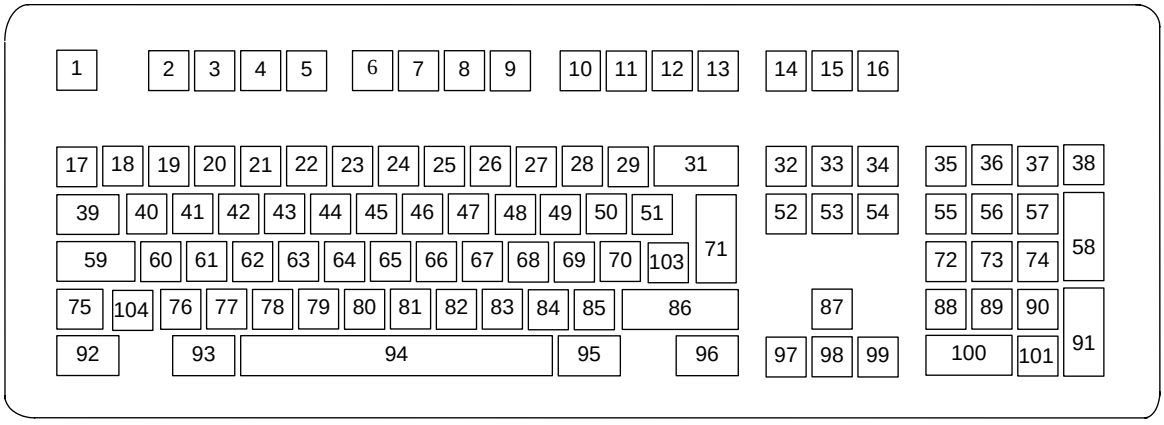


Figure C-4. National (102-Key) Keyboard Key Positions

C.2.3.2 Windows Enhanced Keyboards

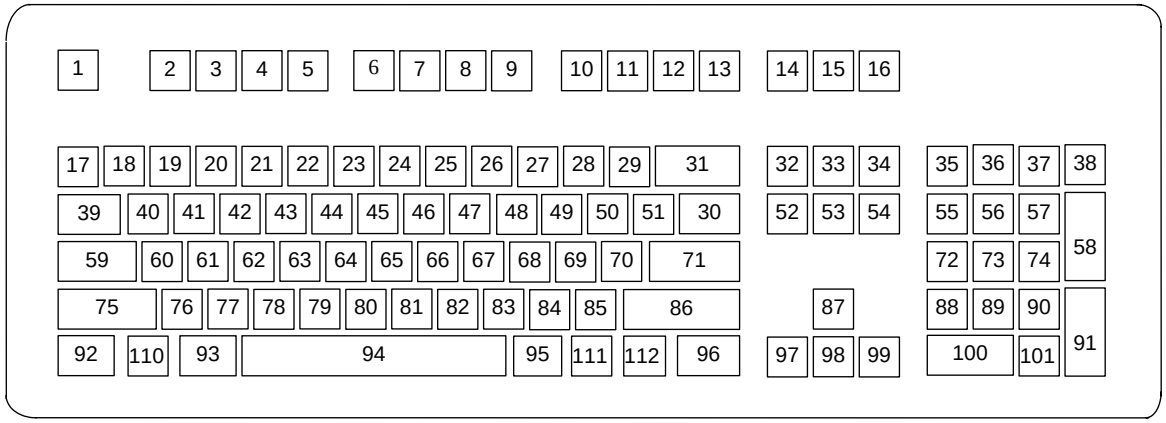


Figure C-5. U.S. English Windows (101W-Key) Keyboard Key Positions

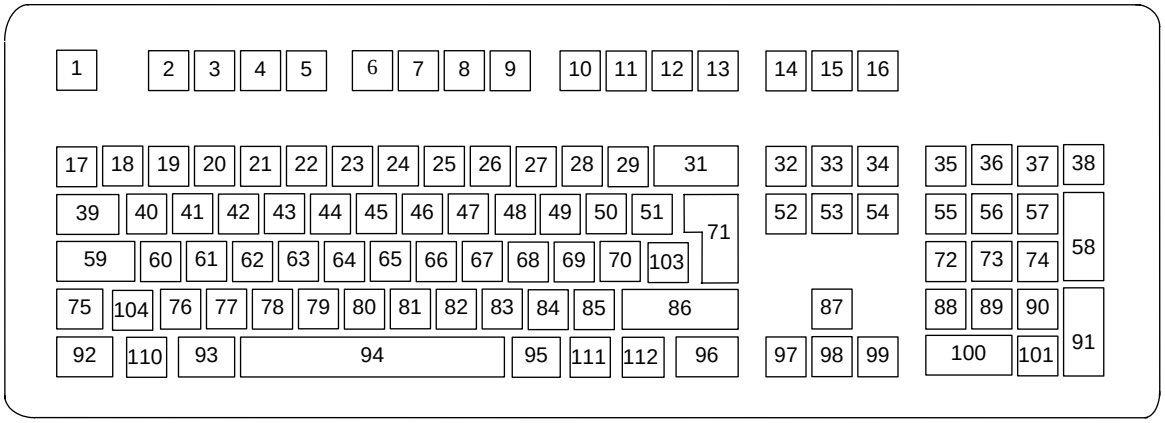
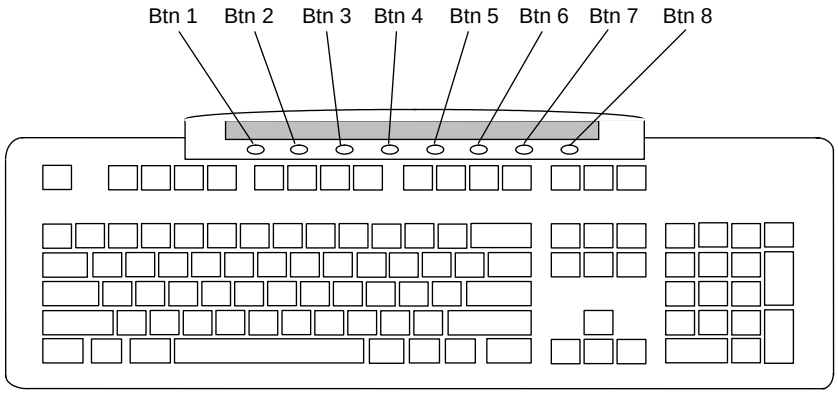


Figure C-6. National Windows (102W-Key) Keyboard Key Positions

C.2.3.3 Easy Access Keyboard

The Easy Access keyboard is a Windows Enhanced-type keyboard that includes special buttons allowing quick internet navigation. The Easy Access Keyboard uses the PS/2-type connection.



Main key positions same as Windows Enhanced (Figures C-5 or C-6).

Figure C-7. 8-Button Easy Access Keyboard Layout

C.2.4 Keys

All keys generate a Make code (when pressed) and a Break code (when released) with the exception of the **Pause** key (pos. 16), which produces a Make code only. All keys with the exception of the **Pause** and Easy Access keys are also typematic, although the typematic action of the **Shift, Ctrl, Alt, Num Lock, Scroll Lock, Caps Lock**, and **Ins** keys is suppressed by the BIOS. Typematic keys, when held down longer than 500 ms, send the Make code repetitively at a 10-12 Hz rate until the key is released. If more than one key is held down, the last key pressed will be typematic.

C.2.4.1 Special Single-Keystroke Functions

The following keys provide the intended function in most applications and environments.

Caps Lock—The **Caps Lock** key (pos. 59), when pressed and released, invokes a BIOS routine that turns on the caps lock LED and shifts into upper case key positions 40-49, 60-68, and 76-82. When pressed and released again, these keys revert to the lower case state and the LED is turned off. Use of the **Shift** key will reverse which state these keys are in based on the **Caps Lock** key.

Num Lock—The **Num Lock** key (pos. 32), when pressed and released, invokes a BIOS routine that turns on the num lock LED and shifts into upper case key positions 55-57, 72-74, 88-90, 100, and 101. When pressed and released again, these keys revert to the lower case state and the LED is turned off.

The following keys provide special functions that require specific support by the application.

Print Scrn—The **Print Scrn** (pos. 14) key can, when pressed, generate an interrupt that initiates a print routine. This function may be inhibited by the application.

Scroll Lock—The **Scroll Lock** key (pos. 15) when pressed and released, invokes a BIOS routine that turns on the scroll lock LED and inhibits movement of the cursor. When pressed and released again, the LED is turned off and the function is removed. This keystroke is always serviced by the BIOS (as indicated by the LED) but may be inhibited or ignored by the application.

Pause—The **Pause** (pos. 16) key, when pressed, can be used to cause the keyboard interrupt to loop, i.e., wait for another key to be pressed. This can be used to momentarily suspend an operation. The key that is pressed to resume operation is discarded. This function may be ignored by the application.

The **Esc**, **Fn** (function), **Insert**, **Home**, **Page Up**/**Down, Delete**, and **End** keys operate at the discretion of the application software.

C.2.4.2 Multi-Keystroke Functions

Shift—The **Shift** key (pos. 75/86), when held down, produces a shift state (upper case) for keys in positions 17-29, 30, 39-51, 60-70, and 76-85 as long as the **Caps Lock** key (pos. 59) is toggled off. If the **Caps Lock** key is toggled on, then a held **Shift** key produces the lower (normal) case for the identified pressed keys. The Shift key also reverses the **Num Lock** state of key positions 55-57, 72, 74, 88-90, 100, and 101.

Ctrl—The **Ctrl** keys (pos. 92/96) can be used in conjunction with keys in positions 1-13, 16, 17-34, 39-54, 60-71, and 76-84. The application determines the actual function. Both **Ctrl** key positions provide identical functionality. The pressed combination of **Ctrl** and **Break** (pos. 16) results in the generation of BIOS function INT 1Bh. This software interrupt provides a method of exiting an application and generally halts execution of the current program.

Alt—The **Alt** keys (pos. 93/95) can be used in conjunction with the same keys available for use with the **Ctrl** keys with the exception that position 14 (**SysRq)** is available instead of position 16 (**Break**). The **Alt** key can also be used in conjunction with the numeric keypad keys (pos. 55-57, 72-74, and 88-90) to enter the decimal value of an ASCII character code from 1-255. The application determines the actual function of the keystrokes. Both **Alt** key positions provide identical functionality. The combination keystroke of **Alt** and **SysRq** results in software interrupt 15h, AX=8500h being executed. It is up to the application to use or not use this BIOS function.

The **Ctrl** and **Alt** keys can be used together in conjunction with keys in positions 1-13, 17-34, 39-54, 60-71, and 76-84. The **Ctrl** and **Alt** key positions used and the sequence in which they are pressed make no difference as long as they are held down at the time the third key is pressed. The **Ctrl**, **Alt**, and **Delete** keystroke combination (required twice if in the Windows environment) initiates a system reset (warm boot) that is handled by the BIOS.

C.2.4.3 Windows Keystrokes

Windows-enhanced keyboards include three additional key positions. Key positions 110 and 111 (marked with the Windows logo) have the same functionality and are used by themselves or in combination with other keys to perform specific “hot-key” type functions for the Windows operating system. The defined functions of the Windows logo keys are listed as follows:

Keystroke	Function
Window Logo	Open Start menu
Window Logo + F1	Display pop-up menu for the selected object
Window Logo + TAB	Activate next task bar button
Window Logo + E	Explore my computer
Window Logo + F	Find document
Window Logo + CTRL + F	Find computer
Window Logo + M	Minimize all
Shift + Window Logo + M	Undo minimize all
Window Logo + R	Display Run dialog box
Window Logo + PAUSE	Perform system function
Window Logo + 0-9	Reserved for OEM use (see following text)

The combination keystroke of the Window Logo + 1-0 keys are reserved for OEM use for auxiliary functions (speaker volume, monitor brightness, password, etc.).

Key position 112 (marked with an application window icon) is used in combination with other keys for invoking Windows application functions.

C.2.4.4 Easy Access Keystrokes

The Easy Access keyboards(Figures C-7) include additional keys (also referred to as buttons) used to streamline internet access and navigation.

These buttons, which can be re-programmed to provide other functions, have the default functionality described below:

8-Button Easy Access Keyboard:

Button #	Description	Default Function
1	Go to favorite web site	Customer web site of choice
2	Go to AltaVista	AltaVista web site
3	Search	AltaVista search engine
4	Check Email	Launches user Email
5	Business Community	Industry specification info
6	Market Monitor	Launches Bloomberg market monitor
7	Meeting Center	Links to user's project center
8	News/PC Lock	News retrieval service

All buttons may be re-programmed by the user through the Easy Access utility.

C.2.5 Keyboard Commands

Table C-1 lists the commands that the keyboard can send to the system (specifically, to the 8042-type logic).

Table C-1.
Keyboard-to-System Commands

Command	Value	Description
Key Detection Error/Over/run	00h [1] FFh [2]	Indicates to the system that a switch closure couldn't be identified.
BAT Completion	AAh	Indicates to the system that the BAT has been successful.
BAT Failure	FCh	Indicates failure of the BAT by the keyboard.
Echo	EEh	Indicates that the Echo command was received by the keyboard.
Acknowledge (ACK)	FAh	Issued by the keyboard as a response to valid system inputs (except the Echo and Resend commands).
Resend	FEh	Issued by the keyboard following an invalid input.
Keyboard ID	83ABh	Upon receipt of the Read ID command from the system, the keyboard issues the ACK command followed by the two IDS bytes.

Note:

[1] Modes 2 and 3.

[2] Mode 1 only.

C.2.6 Scan Codes

The scan codes generated by the keyboard processor are determined by the mode the keyboard is operating in.

- Mode 1: In Mode 1 operation, the keyboard generates scan codes compatible with 8088-/8086-based systems. To enter Mode 1, the scan code translation function of the keyboard controller must be disabled. Since translation is not performed, the scan codes generated in Mode 1 are identical to the codes required by BIOS. Mode 1 is initiated by sending command F0h with the 01h option byte. Applications can obtain system codes and status information by using BIOS function INT 16h with AH=00h, 01h, and 02h.
- Mode 2: Mode 2 is the default mode for keyboard operation. In this mode, the 8042 logic translates the make codes from the keyboard processor into the codes required by the BIOS. This mode was made necessary with the development of the Enhanced III keyboard, which includes additional functions over earlier standard keyboards. Applications should use BIOS function INT 16h, with AH=10h, 11h, and 12h for obtaining codes and status data. In Mode 2, the keyboard generates the Break code, a two-byte sequence that consists of a Make code immediately preceded by F0h (i.e., Break code for 0Eh is “F0h 0Eh”).
- Mode 3: Mode 3 generates a different scan code set from Modes 1 and 2. Code translation must be disabled since translation for this mode cannot be done.

NOTES:

Table C-2.
Keyboard Scan Codes

Key Pos.	Legend	Make/Break Codes (Hex)		
		Mode 1	**Mode 2**	**Mode 3**
1	Esc	01/81	76/F0 76	08/na
2	F1	3B/BB	05/F0 05	07/na
3	F2	3C/BC	06/F0 06	0F/na
4	F3	3D/BD	04/F0 04	17/na
5	F4	3E/BE	0C/F0 0C	1F/na
6	F5	3F/BF	03/F0 03	27/na
7	F6	40/C0	0B/F0 0B	2F/na
8	F7	41/C1	83/F0 83	37/na
9	F8	42/C2	0A/F0 0A	3F/na
10	F9	43/C3	01/FO 01	47/na
11	F10	44/C4	09/F0 09	4F/na
12	F11	57/D7	78/F0 78	56/na
13	F12	58/D8	07/F0 07	5E/na

Table C-2. *(Continued)*
Keyboard Scan Codes

Key Pos.	Legend	Make/Break Codes (Hex)		
		Mode 1	**Mode 2**	**Mode 3**
14	Print Scrn	E0 2A E0 37/E0 B7 E0 AA E0 37/E0 B7 [1] [2] 54/84 [3]	E0 2A E0 7C/E0 F0 7C E0 F0 12 E0 7C/E0 F0 7C [1] [2] 84/F0 84 [3]	57/na
15	Scroll Lock	46/C6	7E/F0 7E	5F/na
16	Pause	E1 1D 45 E1 9D C5/na E0 46 E0 C6/na [3]	E1 14 77 E1 F0 14 F0 77/na E0 7E E0 F0 7E/na [3]	62/na
17	`	29/A9	0E/F0 E0	0E/F0 0E
18	1	02/82	16/F0 16	46/F0 46
19	2	03/83	1E/F0 1E	1E/F0 1E
20	3	04/84	26/F0 26	26/F0 26
21	4	05/85	25/F0 25	25/F0 25
22	5	06/86	2E/F0 2E	2E/F0 2E
23	6	07/87	36/F0 36	36/F0 36
24	7	08/88	3D/F0 3D	3D/F0 3D
25	8	09/89	3E/F0 3E	3E/F0 3E
26	9	0A/8A	46/F0 46	46/F0 46
27	0	0B/8B	45/F0 45	45/F0 45
28	-	0C/8C	4E/F0 4E	4E/F0 4E
29	=	0D/8D	55/F0 55	55/F0 55
30	\	2B/AB	5D/F0 5D	5C/F0 5C
31	Backspace	0E/8E	66/F0 66	66/F0 66
32	Insert	E0 52/E0 D2 E0 AA E0 52/E0 D2 E0 2A [4] E0 2A E0 52/E0 D2 E0 AA [6]	E0 70/E0 F0 70 E0 F0 12 E0 70/E0 F0 70 E0 12 [5] E0 12 E0 70/E0 F0 70 E0 F0 12 [6]	67/na
33	Home	E0 47/E0 D2 E0 AA E0 52/E0 D2 E0 2A [4] E0 2A E0 47/E0 C7 E0 AA [6]	E0 6C/E0 F0 6C E0 F0 12 E0 6C/E0 F0 6C E0 12 [5] E0 12 E0 6C/E0 F0 6C E0 F0 12 [6]	6E/na
34	Page Up	E0 49/E0 C7 E0 AA E0 49/E0 C9 E0 2A [4] E0 2A E0 49/E0 C9 E0 AA [6]	E0 7D/E0 F0 7D E0 F0 12 E0 7D/E0 F0 7D E0 12 [5] E0 12 E0 7D/E0 F0 7D E0 F0 12 [6]	6F/na

Table C-2. *(Continued)*
Keyboard Scan Codes

Key Pos.	Legend	Make/Break Codes (Hex)		
		Mode 1	**Mode 2**	**Mode 3**
35	Num Lock	45/C5	77/F0 77	76/na
36	/	E0 35/E0 B5 E0 AA E0 35/E0 B5 E0 2A [1]	E0 4A/E0 F0 4A E0 F0 12 E0 4A/E0 F0 4A E0 12 [1]	77/na
37	*	37/B7	7C/F0 7C	7E/na
38	-	4A/CA	7B/F0 7B	84/na
39	Tab	0F/8F	0D/F0 0D	0D/na
40	Q	10/90	15/F0 15	15/na
41	W	11/91	1D/F0 1D	1D/F0 1D
42	E	12/92	24/F0 24	24/F0 24
43	R	13/93	2D/F0 2D	2D/F0 2D
44	T	14/94	2C/F0 2C	2C/F0 2C
45	Y	15/95	35/F0 35	35/F0 35
46	U	16/96	3C/F0 3C	3C/F0 3C
47	I	17/97	43/F0 43	43/F0 43
48	O	18/98	44/F0 44	44/F0 44
49	P	19/99	4D/F0 4D	4D/F0 4D
50	[	1A/9A	54/F0 54	54/F0 54
51	]	1B/9B	5B/F0 5B	5B/F0 5B
52	Delete	E0 53/E0 D3 E0 AA E0 53/E0 D3 E0 2A [4] E0 2A E0 53/E0 D3 E0 AA [6]	E0 71/E0 F0 71 E0 F0 12 E0 71/E0 F0 71 E0 12 [5] E0 12 E0 71/E0 F0 71 E0 F0 12 [6]	64/F0 64
53	End	E0 4F/E0 CF E0 AA E0 4F/E0 CF E0 2A [4] E0 2A E0 4F/E0 CF E0 AA [6]	E0 69/E0 F0 69 E0 F0 12 E0 69/E0 F0 69 E0 12 [5] E0 12 E0 69/E0 F0 69 E0 F0 12 [6]	65/F0 65
54	Page Down	E0 51/E0 D1 E0 AA E0 51/E0 D1 E0 2A [4] E0 @a E0 51/E0 D1 E0 AA [6]	E0 7A/E0 F0 7A E0 F0 12 E0 7A/E0 F0 7A E0 12 [5] E0 12 E0 7A/E0 F0 7A E0 F0 12 [6]	6D/F0 6D
55	7	47/C7 [6]	6C/F0 6C [6]	6C/na [6]
56	8	48/C8 [6]	75/F0 75 [6]	75/na [6]
57	9	49/C9 [6]	7D/F0 7D [6]	7D/na [6]

Table C-2. *(Continued)*
Keyboard Scan Codes

Key Pos.	Legend	Make/Break Codes (Hex)		
		Mode 1	**Mode 2**	**Mode 3**
58	+	4E/CE [6]	79/F0 79 [6]	7C/F0 7C
59	Caps Lock	3A/BA	58/F0 58	14/F0 14
60	A	1E/9E	1C/F0 1C	1C/F0 1C
61	S	1F/9F	1B/F0 1B	1B/F0 1B
62	D	20/A0	23/F0 23	23/F0 23
63	F	21/A1	2B/F0 2B	2B/F0 2B
64	G	22/A2	34/F0 34	34/F0 34
65	H	23/A3	33/F0 33	33/F0 33
66	J	24/A4	3B/F0 3B	3B/F0 3B
67	K	25/A5	42/F0 42	42/F0 42
68	L	26/A6	4B/F0 4B	4B/F0 4B
69	;	27/A7	4C/F0 4C	4C/F0 4C
70	‘	28/A8	52/F0 52	52/F0 52
71	Enter	1C/9C	5A/F0 5A	5A/F0 5A
72	4	4B/CB [6]	6B/F0 6B [6]	6B/na [6]
73	5	4C/CC [6]	73/F0 73 [6]	73/na [6]
74	6	4D/CD [6]	74/F0 74 [6]	74/na [6]
75	Shift (left)	2A/AA	12/F0 12	12/F0 12
76	Z	2C/AC	1A/F0 1A	1A/F0 1A
77	X	2D/AD	22/F0 22	22/F0 22
78	C	2E/AE	21/F0 21	21/F0 21
79	V	2F/AF	2A/F0 2A	2A/F0 2A
80	B	30/B0	32/F0 32	32/F0 32
81	N	31/B1	31/F0 31	31/F0 31
82	M	32/B2	3A/F0 3A	3A/F0 3A
83	,	33/B3	41/F0 41	41/F0 41
84	.	34/B4	49/F0 49	49/F0 49

Table C-2. *(Continued)*
Keyboard Scan Codes

Key Pos.	Legend	Make/Break Codes (Hex)		
		Mode 1	**Mode 2**	**Mode 3**
85	/	35/B5	4A/F0 4A	4A/F0 4A
86	Shift (right)	36/B6	59/F0 59	59/F0 59
87		E0 48/E0 C8 E0 AA E0 48/E0 C8 E0 2A [4] E0 2A E0 48/E0 C8 E0 AA [6]	E0 75/E0 F0 75 E0 F0 12 E0 75/E0 F0 75 E0 12 [5] E0 12 E0 75/E0 F0 75 E0 F0 12 [6]	63/F0 63
88	1	4F/CF [6]	69/F0 69 [6]	69/na [6]
89	2	50/D0 [6]	72/F0 72 [6]	72/na [6]
90	3	51/D1 [6]	7A/F0 7A [6]	7A/na [6]
91	Enter	E0 1C/E0 9C	E0 5A/F0 E0 5A	79/F0 79[6]
92	Ctrl (left)	1D/9D	14/F0 14	11/F0 11
93	Alt (left)	38/B8	11/F0 11	19/F0 19
94	(Space)	39/B9	29/F0 29	29/F0 29
95	Alt (right)	E0 38/E0 B8	E0 11/F0 E0 11	39/na
96	Ctrl (right)	E0 1D/E0 9D	E0 14/F0 E0 14	58/na
97		E0 4B/E0 CB E0 AA E0 4B/E0 CB E0 2A [4] E0 2A E0 4B/E0 CB E0 AA [6]	E0 6B/Eo F0 6B E0 F0 12 E0 6B/E0 F0 6B E0 12[5] E0 12 E0 6B/E0 F0 6B E0 F0 12[6]	61/F0 61
98		E0 50/E0 D0 E0 AA E0 50/E0 D0 E0 2A [4] E0 2A E0 50/E0 D0 E0 AA [6]	E0 72/E0 F0 72 E0 F0 12 E0 72/E0 F0 72 E0 12[5] E0 12 E0 72/E0 F0 72 E0 F0 12[6]	60/F0 60
99		E0 4D/E0 CD E0 AA E0 4D/E0 CD E0 2A [4] E0 2A E0 4D/E0 CD E0 AA [6]	E0 74/E0 F0 74 E0 F0 12 E0 74/E0 F0 74 E0 12[5] E0 12 E0 74/E0 F0 74 E0 F0 12[6]	6A/F0 6A
100	0	52/D2 [6]	70/F0 70 [6]	70/na [6]
101	.	53/D3 [6]	71/F0 71 [6]	71/na [6]
102	na	7E/FE	6D/F0 6D	7B/F0 7B
103	na	2B/AB	5D/F0 5D	53/F0 53
104	na	36/D6	61/F0 61	13/F0 13

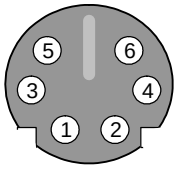
Table C-2. *(Continued)*
Keyboard Scan Codes

Key Pos.	Legend	Make/Break Codes (Hex)		
		Mode 1	**Mode 2**	**Mode 3**
110	(Win95) [7]	E0 5B/E0 DB E0 AA E0 5B/E0 DB E0 2A [4] E0 2A E0 5B/E0 DB E0 AA [6]	E0 1F/E0 F0 1F E0 F0 12 E0 1F/E0 F0 1F E0 12 [5] E0 12 E0 1F/E0 F0 1F E0 F0 12 [6]	8B/F0 8B
111	(Win95) [7]	E0 5C/E0 DC E0 AA E0 5C/E0 DC E0 2A [4] E0 2A E0 5C/E0 DC E0 AA [6]	E0 2F/E0 F0 27 E0 F0 12 E0 27/E0 F0 27 E0 12 [5] E0 12 E0 27/E0 F0 27 E0 F0 12 [6]	8C/F0 8C
112	(Win Apps) [7]	E0 5D/E0 DD E0 AA E0 5D/E0 DD E0 2A [4] E0 2A E0 5D E0 DD E0 AA [6]	E0 2F/E0 F0 2F E0 F0 12 E0 2F/E0 F0 2F E0 12 [5] E0 12 E0 2F/E0 F0 2F E0 F0 12 [6	8D/F0 8D
Btn 1	[8]	E0 1E/E0 9E	E0 1C/E0 F0 1C	95/F0 95
Btn 2	[8]	E0 26/E0 A6	E0 4B/E0 F0 4B	9C/F0 9C
Btn 3	[8]	E0 25/E0 A5	E0 42/E0 F0 42	9D/F0 9D
Btn 4	[8]	E0 23/E0 A3	E0 33/E0 F0 33	9A/F0 9A
Btn 5	[8]	E0 21/E0 A1	E0 2B/E0 F0 2B	99/F0 99
Btn 6	[8]	E0 12/E0 92	E0 24/E0 F0 24	96/F0 96
Btn 7	[8]	E0 32/E0 B2	E0 3A/E0 F0 3A	97/F0 97
Btn 1	[9]	E0 23/E0 A3	E0 33/E0 F0 33	9A/F0 9A
Btn 2	[9]	E0 1F/E0 9F	E0 1B/E0 F0 1B	80/F0 80
Btn 3	[9]	E0 1A/E0 9A	E0 54/E0 F0 54	99/F0 99
Btn 4	[9]	E0 1E/E0 9E	E0 1C/E0 F0 1C	95/F0 95
Btn 5	[9]	E0 13/E0 93	E0 2D/E0 F0 2D	0C/F0 0C
Btn 6	[9]	E0 14/E0 94	E0 2C/E0 F0 2C	9D/F0 9D
Btn 7	[9]	E0 15/E0 95	E0 35/E0 F0 35	96/F0 96
Btn 8	[9]	E0 1B/E0 9B	E0 5B/E0 F0 5B	97/F0 97

All codes assume Shift, Ctrl, and Alt keys inactive unless otherwise noted.
NA = Not applicable
[1] Shift (left) key active.
[2] Ctrl key active.
[3] Alt key active.
[4] Left Shift key active. For active right Shift key, substitute AA/2A make/break codes for B6/36 codes.
[5] Left Shift key active. For active right Shift key, substitute F0 12/12 make/break codes for F0 59/59 codes.
[6] Num Lock key active.
[7] Windows keyboards only.
[8] 7-Button Easy Access keyboard.
[9] 8-Button Easy Access keyboard.

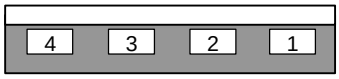
C.3 Connectors

Two types of keyboard interfaces may be used in HP/Compaq systems: PS/2-type and USB-type. System units that provide a PS/2 connector will ship with a PS/2-type keyboard but may also support simultaneous connection of a USB keyboard. Systems that do not provide a PS/2 interface will ship with a USB keyboard. For a detailed description of the PS/2 and USB interfaces refer to Chapter 5 “Input/Output” of this guide. The keyboard cable connectors and their pinouts are described in the following figures:



Pin	Function
1	Data
2	Not connected
3	Ground
4	+5 VDC
5	Clock
6	Not connected

Figure C-9. PS/2 Keyboard Cable Connector (Male)



Pin	Function
1	+5 VDC
2	Data (-)
3	Data (+)
4	Ground

Figure C-10. USB Keyboard Cable Connector (Male)

Index

S

T

U

V

W