

# Mixing Intel® 32-bit processors in ProLiant servers

technology brief



Abstract.....	2
Introduction.....	2
Basic issues.....	2
Testing.....	2
Processor steppings.....	3
Intel support for mixed steppings.....	3
OS support for mixed steppings.....	4
Support for mixing processors in ProLiant servers.....	4
General processor architecture.....	4
General mixing guidelines.....	4
Dual- and four-way multiprocessor servers.....	5
Eight-way multiprocessor servers.....	5
Conclusion.....	5
For more information.....	6
Call to action.....	6

## Abstract

To ensure full protection and support under manufacturer warranties, users must configure computer hardware and software according to manufacturer guidelines. In the case of Intel 32-bit processors designed for use in a server, guidelines of the processor manufacturer, the server manufacturer, and the operating system vendor must be reconciled.

This technology brief identifies basic issues of mixing Intel 32-bit processors with different frequencies, cache sizes, or steppings. Intel supports mixed steppings only under certain conditions. The major operating system vendors support mixed steppings of processors under the same conditions as those listed by Intel. All ProLiant multiprocessor servers support mixed steppings of Intel 32-bit processors. Certain ProLiant multiprocessor servers allow mixing cache size and frequency of processors, according to the general guidelines given within this brief.

Information in this technology brief refers to the 6th- and 7th-generation 32-bit processors from Intel.

## Introduction

Intel Corporation's 32-bit server processor line includes several families of processors with varying core frequencies, level 2 (L2) cache sizes, and steppings. The 6th-generation processor architecture included several successive families: the Pentium Pro, Pentium® II, Pentium III, Pentium II Xeon, and Pentium III Xeon. In late 2000, Intel introduced its NetBurst (7th-generation) architecture in the 32-bit line, which includes the Xeon and the Xeon MP processors.<sup>1</sup>

The purpose of this technology brief is to identify key issues regarding 32-bit processor mixing and to explain support for processor mixing in ProLiant industry-standard servers. This brief is written with the assumption that the reader is familiar with basic processor technology.

## Basic issues

To ensure full protection and support under manufacturer warranties, users must configure computer hardware and software according to manufacturer guidelines. In the case of processors for use in servers, guidelines of multiple vendors must be reconciled: those of the processor manufacturer, the server manufacturer, and the operating system (OS) vendor. The question of vendor support for processor mixing is clouded by differences in vendor testing programs and vague wording of vendor support policies.

## Testing

With the rapid introduction of new processors and the race to bring new products to market, no vendor has sufficient time and resources to test every possible combination of mixed processors for all potential problems. Intel conducts its own testing program for the processors it markets and publishes identified errata and workarounds on the Intel website. For compatibility testing through its Windows Hardware Quality Labs (WHQL) and certification through the Microsoft® Windows Logo Program for hardware, Microsoft Corporation requires that systems meet defined processor configuration restrictions.<sup>2</sup> Other OS vendors may also have their own qualification procedures for multiprocessor servers.

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<sup>1</sup> For more information about Intel processors, see the technology brief titled *the Intel microprocessor roadmap for industry-standard servers*, document number TC40504TB, at <http://h200006.www2.hp.com/bc/docs/support/SupportManual/c00164255/c00164255.pdf>.

<sup>2</sup> For up-to-date information about the Microsoft Windows Logo Program, refer to the Microsoft website at [www.microsoft.com](http://www.microsoft.com).

Server manufacturers and users are free to do additional validation of mixed processor configurations if they choose. HP has performed testing for certain server configurations. To determine if a specific ProLiant server allows mixed frequency and cache size processors, refer to the HP website at: <http://h18000.www1.hp.com/products/servers/processor-mixing/>.

## Processor steppings

Processor steppings are versions of the same processor model (for example, the Intel Pentium III Xeon processor) that vary only slightly, usually to improve performance or manufacturing yield. Each stepping requires changes to the system ROM. For each processor stepping that it produces, Intel provides a microcode patch for inclusion in the system ROM. Each Intel processor stepping has a unique CPU ID, and its microcode patch contains that same CPU ID. Within the system ROM there is a table where the microcode patches are stored. Server vendors must continually add newly-released Intel patches to keep their ROMs up to date.

HP allows N+n steppings; that is, a customer can upgrade to processors that are more than one level higher in stepping.

For example, if a customer has a four-way ProLiant server containing two processors and decides to add two more processors, the new processors could be of a different stepping. The current system ROM may not contain the correct microcode patch for the two new processors.<sup>3</sup> Customers should flash the ROM on that server using an updated ROMPaq before installing the new processors. If this is not done, the ROM may generate the following error message to prevent the user from operating the processor with the wrong microcode:

UNSUPPORTED PROCESSOR DETECTED SYSTEM HALTED

After a processor has been installed, stepping identification can be problematic for customers because a heat sink typically covers the top of the processor chip. Utilities provided with operating systems may be of help. For example under Windows NT, a system administrator can use the Windows NT Diagnostics utility to identify the stepping level of each installed processor. Alternatively, a system administrator can use Survey Utility to view the steppings of installed processors. Copies of Survey Utility are distributed as part of the ProLiant Essentials Foundation Pack. The utility can also be downloaded for a specific ProLiant server from the Support and Drivers web pages at [www.hp.com](http://www.hp.com).

## Intel support for mixed steppings

Based on the information available on the Intel website at the time of this writing<sup>4</sup>, Intel supports mixed steppings of processors only under these conditions:

- All processors in a system must have identical family and model numbers as indicated by the CPU ID instruction.
- All processors in a system must operate at the same frequency; that is, at the highest frequency rating commonly supported by all the processors.
- All processors in a system must have the same cache size.
- The processor with the lowest feature set (stepping) must be the bootstrap processor.

Note also that for the Pentium II Xeon and Pentium III Xeon processors, Intel does not support the Functional Redundancy Checking Mode (FRC mode) in servers using a master and checker pair of processors with different steppings.

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<sup>3</sup> For some generation 2 ProLiant servers, the customer may install the processors before flashing the ROM. The ROM will generate a message that the system will only boot a ROMPaq disk.

<sup>4</sup> Consult the Intel website for complete and up-to-date information about Intel's support of processor mixing.

## OS support for mixed steppings

Like Intel, OS vendors support mixing processors only if all processors in a system have identical family and model numbers, operate at the same frequency, and have the same cache size, and if the processor with the lowest feature set is the bootstrap processor. Statements from OS vendors tend to be vague about support for mixed processor steppings. Typically, major operating systems do not contain code that inhibits operation of servers containing multiple processors with different steppings.

## Support for mixing processors in ProLiant servers

ProLiant servers support mixed steppings of Intel processors through their use of highly integrated hardware and system ROM code. Moreover, through its internal testing, HP allows specific ProLiant servers to be configured with processors of mixed cache sizes and mixed frequencies.

### General processor architecture

Intel has designed the Pentium II, Pentium III, and the Xeon processors differently in their ability to change operating frequency:

- Pentium II and III processors are locked to the frequency ratio at which Intel intends them to run. Since they are frequency locked, Pentium II and Pentium III processors with different frequencies cannot be mixed in ProLiant servers.
- Intel Xeon processors are also speed-locked to the frequency at which Intel intends them to run. Xeon processors with different frequencies **cannot** be mixed in ProLiant servers.
- Pentium II Xeon and Pentium III Xeon processors, on the other hand, are designed as speed-limited processors which can be used in mixed frequencies and cache sizes; however, there are two exceptions. First, the 500/550 MHz Pentium III Xeon processors **cannot** be mixed with 700-MHz or higher-frequency Pentium III Xeon processors. Also, the core frequency for the 900 MHz Pentium III Xeon processors is locked so that the 900-MHz Pentium III Xeon processors cannot be mixed with any other Pentium III Xeon processors.
- Xeon MP processors are also speed-limited. This means, for example, that a 2.0-GHz Xeon MP processor, if it were mixed with a 1.5-GHz Xeon MP processor, would be slowed down to match the 1.5-GHz operating frequency.

### General mixing guidelines

ProLiant dual-way, four-way and eight-way multiprocessing servers are each designed using the most suitable processor and with their own mixing guidelines. For any ProLiant server to use mixed processor frequencies or cache sizes, all processors in the server must be of the same processor family and model. This means, for example, that Pentium II Xeon processors **cannot** be mixed with Pentium III Xeon processors.

For ProLiant servers that allow mixed frequencies and cache sizes, the processor frequency is automatically downgraded by the system ROM to the speed of the slowest processor. The ROM also automatically determines which processor is the lowest stepping and sets it as the bootstrap processor, regardless of the physical location of the processor.<sup>5</sup>

To determine if a specific ProLiant server allows mixed frequency and cache size processors, refer to the HP website at: <http://h18000.www1.hp.com/products/servers/processor-mixing/>

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<sup>5</sup> In some Generation 1 ProLiant servers, the customer had to identify the processor with the lowest stepping and insert it as the bootstrap (P1) processor.

### **Dual- and four-way multiprocessor servers**

Dual-processor servers support mixed steppings, but they do not allow mixed frequency or mixed cache sizes. Stepping identification can be determined normally through ProLiant utilities such as Survey Utility, or through the operating system utilities.

Four-way servers that use the Pentium Pro, the Pentium II Xeon, or the Pentium III Xeon processor can allow mixed frequencies and cache sizes (with the exceptions noted previously for Pentium III Xeon). Refer to the website at <http://h18000.www1.hp.com/products/servers/processor-mixing/> for specific servers that allow processor mixing.

For a ProLiant server containing mixed processors to operate correctly, the user may be required to flash the ROM before installing new processors. The latest ROM is available at this URL: <http://h18023.www1.hp.com/support/files/server/us/index.html>.

### **Eight-way multiprocessor servers**

ProLiant eight-way servers using the Pentium Pro and the Pentium III Xeon processors also support frequency and cache size mixing of processors.

When using Pentium III Xeon processors with different cache sizes, the processors must be installed in pairs that have the same cache size: the first pair in slot 1 and Slot 2; the second pair in Slot 3 and Slot 4; the third pair in slot 5 and Slot 6; and the fourth pair in Slot 7 and Slot 8.

For a ProLiant server containing mixed processors to operate correctly, the user may be required to flash the ROM before installing new processors. The latest ROM is available at this URL: <http://h18023.www1.hp.com/support/files/server/us/index.html>.

## **Conclusion**

ProLiant servers that allow mixed processors undergo extensive internal testing to help protect customer investments in their existing processors. That testing has identified no errata affecting the proper operation of ProLiant servers containing processors with mixed steppings or mixed cache sizes, when configured according to the guidelines provided in this brief and on the ProLiant web pages. If a customer's server requirements include certification through the Microsoft WHQL program, however, the customer should not mix cache sizes in ProLiant servers.

## For more information

[www.hp.com/go/proliant](http://www.hp.com/go/proliant)

HP ProLiant servers website

## Call to action

To help us better understand and meet your needs for ISS technology information, please send comments about this paper to: [TechCom@HP.com](mailto:TechCom@HP.com).

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