Technical Reference Guide

HP Compaq dc7800 Series Business Desktop Computers

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This document provides information on the design, architecture, function, and capabilities of the HP Compaq dc7800 Series Business Desktop Computers. This information may be used by engineers, technicians, administrators, or anyone needing detailed information on the products covered.

Technical Reference Guide

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First Edition (October 2007)

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1 Introduction

1.1 About this Guide

This guide provides technical information about HP Compaq dc7800 Business PC personal computers that feature Intel processors and the Intel Q35 Express chipset. This document describes in detail the system's design and operation for programmers, engineers, technicians, and system administrators, as well as end-users wanting detailed information.

The chapters of this guide primarily describe the hardware and firmware elements and primarily deal with the system board and the power supply assembly. The appendices contain general data such as error codes and information about standard peripheral devices such as keyboards, graphics cards, and communications adapters.

This guide can be used either as an online document or in hardcopy form.

1.1.1 Online Viewing

Online viewing allows for quick navigating and convenient searching through the document. A color monitor will also allow the user to view the color shading used to highlight differential data. A softcopy of the latest edition of this guide is available for downloading in .pdf file format at the following URL: www.hp.com

Viewing the file requires a copy of Adobe Acrobat Reader available at no charge from Adobe Systems, Inc. at the following URL: www.adobe.com

1.1.2 Hardcopy

A hardcopy of this guide may be obtained by printing from the .pdf file. The document is designed for printing in an 8 ½ x 11-inch format.

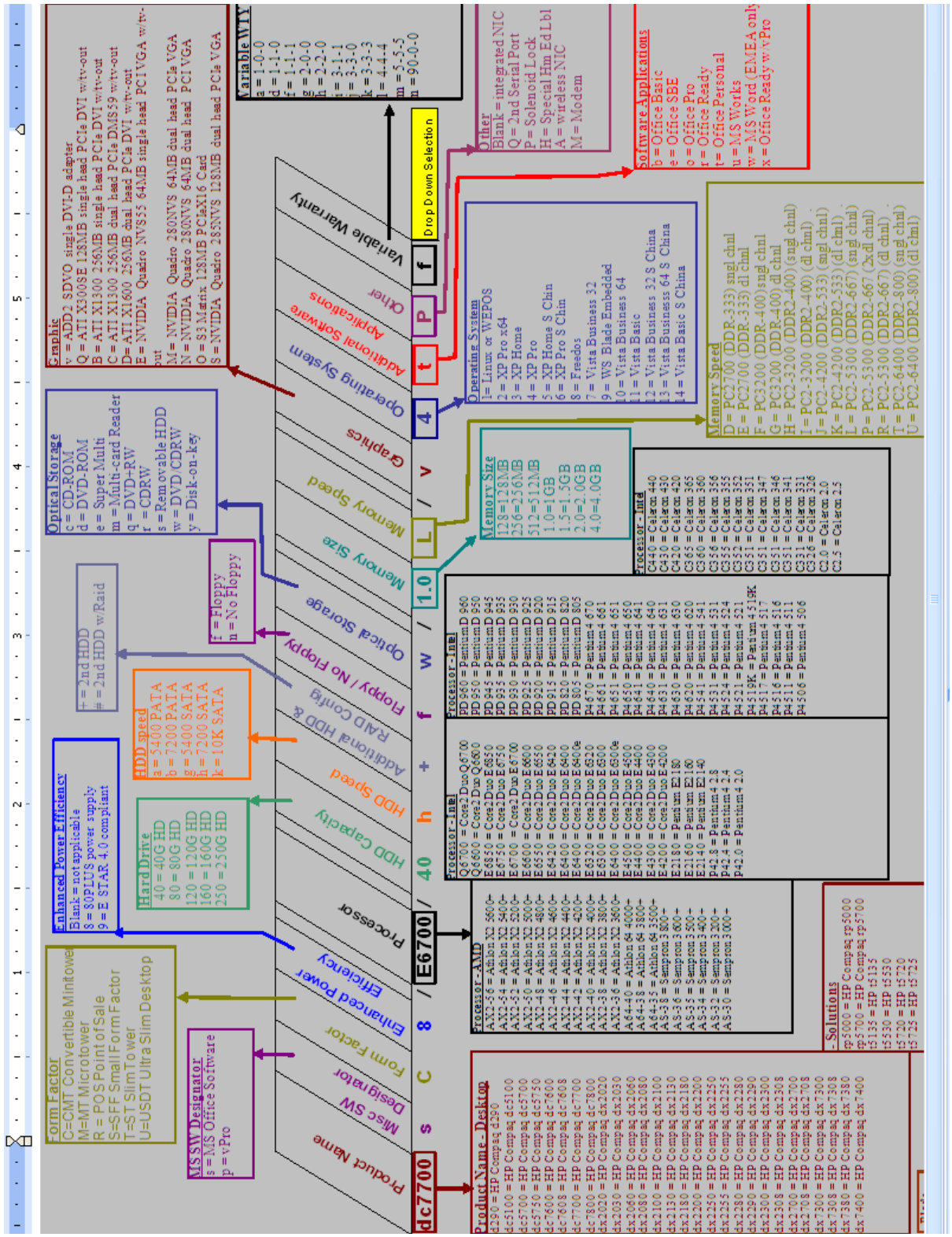
1.2 Additional Information Sources

For more information on components mentioned in this guide refer to the indicated manufacturers' documentation, which may be available at the following online sources:

- HP Corporation: www.hp.com
- Intel Corporation: www.intel.com
- Standard Microsystems Corporation: www.smsc.com
- Serial ATA International Organization (SATA-IO): www.serialATA.org.
- USB user group: www.usb.org

1.3 Model Numbering Convention

The current model numbering convention for HP systems is shown as follows:


dc7700
Product Name
Misc SW
Designator
Form Factor
Enhanced Power
Efficiency
Processor
HDD Capacity
HDD Speed
Additional HDD &
RAID Config
Floppy / No Floppy
Optical Storage
Memory Size
Memory Speed
Graphics
Operating System
Additional Software
Applications
Other
Variable Warranty
Drop Down Selection
s C 8 / E6700 / 40 h + f w / 1.0 L / v 4 t P f
Product Name - Desktop
Form Factor
Enhanced Power Efficiency
Hard Drive
HDD speed
Optical Storage
Graphic
Variable WTY
Operating System
Memory Size
Processor - Intel
Processor - AMD
Memory Speed
Software Applications
Other
- Solutions

1.4 Serial Number

The serial number is located on a sticker placed on the exterior cabinet. The serial number is also written into firmware and may be read with HP Diagnostics or Insight Manager utilities.

1.5 Notational Conventions

The notational guidelines used in this guide are described in the following subsections.

1.5.1 Special Notices

The usage of warnings, cautions, and notes is described as follows:

WARNING: Text set off in this manner indicates that failure to follow directions could result in bodily harm or loss of life.

CAUTION: Text set off in this manner indicates that failure to follow directions could result in damage to equipment or loss of information.

Text set off in this manner provides information that may be helpful.

1.5.2 Values

Differences between bytes and bits are indicated as follows:

MB = megabytes

Mb = megabits

1.5.3 Ranges

Ranges or limits for a parameter are shown using the following methods:

Example A:	Bits <7..4> = bits 7, 6, 5, and 4.
Example B:	IRQ3-7, 9 = IRQ signals 3 through 7, and IRQ signal 9

1.6 Common Acronyms and Abbreviations

Table 1-1 lists the acronyms and abbreviations used in this guide.

Table 1-1
Acronyms and Abbreviations

Acronym or Abbreviation	Description
A	ampere
AC	alternating current
ACPI	Advanced Configuration and Power Interface
A/D	analog-to-digital
ADC	Analog-to-digital converter
ADD or ADD2	Advanced digital display (card)
AGP	Accelerated graphics port
API	application programming interface
APIC	Advanced Programmable Interrupt Controller
APM	advanced power management
AOL	Alert-On-LAN™
ASIC	application-specific integrated circuit
ASF	Alert Standard Format
AT	1. attention (modem commands) 2. 286-based PC architecture
ATA	AT attachment (IDE protocol)
ATAPI	ATA w/packet interface extensions
AVI	audio-video interleaved
AVGA	Advanced VGA
AWG	American Wire Gauge (specification)
BAT	Basic assurance test
BCD	binary-coded decimal
BIOS	basic input/output system
bis	second/new revision
BNC	Bayonet Neill-Concelman (connector type)
bps or b/s	bits per second
BSP	Bootstrap processor
BTO	Built to order
CAS	column address strobe
CD	compact disk
CD-ROM	compact disk read-only memory
CDS	compact disk system
CGA	color graphics adapter

Table 1-1 *(Continued)*
Acronyms and Abbreviations

Acronym or Abbreviation	Description
Ch	Channel, chapter
cm	centimeter
CMC	cache/memory controller
CMOS	complimentary metal-oxide semiconductor (configuration memory)
Cntlr	controller
Cntrl	control
codec	1. coder/decoder 2. compressor/decompressor
CPQ	Compaq
CPU	central processing unit
CRIMM	Continuity (blank) RIMM
CRT	cathode ray tube
CSM	1. Compaq system management 2. Compaq server management
DAC	digital-to-analog converter
DC	direct current
DCH	DOS compatibility hole
DDC	Display Data Channel
DDR	Double data rate (memory)
DIMM	dual inline memory module
DIN	Deutche IndustriNorm (connector type)
DIP	dual inline package
DMA	direct memory access
DMI	Desktop management interface
dpi	dots per inch
DRAM	dynamic random access memory
DRQ	data request
DVI	Digital video interface
dword	Double word (32 bits)
EDID	extended display identification data
EDO	extended data out (RAM type)
EEPROM	electrically erasable PROM
EGA	enhanced graphics adapter
EIA	Electronic Industry Association
EISA	extended ISA
EPP	enhanced parallel port
EIDE	enhanced IDE

Table 1-1 *(Continued)*
Acronyms and Abbreviations

Acronym or Abbreviation	Description
ESCD	Extended System Configuration Data (format)
EV	Environmental Variable (data)
ExCA	Exchangeable Card Architecture
FIFO	first in/first out
FL	flag (register)
FM	frequency modulation
FPM	fast page mode (RAM type)
FPU	Floating point unit (numeric or math coprocessor)
FPS	Frames per second
ft	Foot/feet
GB	gigabyte
GMCH	Graphics/memory controller hub
GND	ground
GPIO	general purpose I/O
GPOC	general purpose open-collector
GART	Graphics address re-mapping table
GUI	graphic user interface
h	hexadecimal
HW	hardware
hex	hexadecimal
Hz	Hertz (cycles-per-second)
ICH	I/O controller hub
IDE	integrated drive element
IEEE	Institute of Electrical and Electronic Engineers
IF	interrupt flag
I/F	interface
IGC	integrated graphics controller
in	inch
INT	interrupt
I/O	input/output
IPL	initial program loader
IrDA	Infrared Data Association
IRQ	interrupt request
ISA	industry standard architecture

Table 1-1 *(Continued)*
Acronyms and Abbreviations

Acronym or Abbreviation	Description
Kb/KB	kilobits/kilobytes (x 1024 bits/x 1024 bytes)
Kb/s	kilobits per second
kg	kilogram
KHz	kilohertz
kV	kilovolt
lb	pound
LAN	local area network
LCD	liquid crystal display
LED	light-emitting diode
LPC	Low pin count
LSI	large scale integration
LSb/LSB	least significant bit/least significant byte
LUN	logical unit (SCSI)
m	Meter
MCH	Memory controller hub
MMX	multimedia extensions
MPEG	Motion Picture Experts Group
ms	millisecond
MSb/MSB	most significant bit/most significant byte
mux	multiplex
MVA	motion video acceleration
MVW	motion video window
n	variable parameter/value
NIC	network interface card/controller
NiMH	nickel-metal hydride
NMI	non-maskable interrupt
NRZI	Non-return-to-zero inverted
ns	nanosecond
NT	nested task flag
NTSC	National Television Standards Committee
NVRAM	non-volatile random access memory
OS	operating system
PAL	1. programmable array logic 2. phase alternating line
PATA	Parallel ATA

Table 1-1 *(Continued)*
Acronyms and Abbreviations

Acronym or Abbreviation	Description
PC	Personal computer
PCA	Printed circuit assembly
PCI	peripheral component interconnect
PCI-E	PCI Express
PCM	pulse code modulation
PCMCIA	Personal Computer Memory Card International Association
PEG	PCI express graphics
PFC	Power factor correction
PIN	personal identification number
PIO	Programmed I/O
PN	Part number
POST	power-on self test
PROM	programmable read-only memory
PTR	pointer
RAID	Redundant array of inexpensive disks (drives)
RAM	random access memory
RAS	row address strobe
rcvr	receiver
RDRAM	(Direct) Rambus DRAM
RGB	red/green/blue (monitor input)
RH	Relative humidity
RMS	root mean square
ROM	read-only memory
RPM	revolutions per minute
RTC	real time clock
R/W	Read/Write
SATA	Serial ATA
SCSI	small computer system interface
SDR	Singles data rate (memory)
SDRAM	Synchronous Dynamic RAM
SDVO	Serial digital video output
SEC	Single Edge-Connector
SECAM	sequential colour avec memoire (sequential color with memory)
SF	sign flag

Table 1-1 *(Continued)*
Acronyms and Abbreviations

Acronym or Abbreviation	Description
SGRAM	Synchronous Graphics RAM
SIMD	Single instruction multiple data
SIMM	single in-line memory module
SMART	Self Monitor Analysis Report Technology
SMI	system management interrupt
SMM	system management mode
SMRAM	system management RAM
SPD	serial presence detect
SPDIF	Sony/Philips Digital Interface (IEC-958 specification)
SPN	Spare part number
SPP	standard parallel port
SRAM	static RAM
SSE	Streaming SIMD extensions
STN	super twist pneumatic
SVGA	super VGA
SW	software
TAD	telephone answering device
TAFI	Temperature-sensing And Fan control Integrated circuit
TCP	tape carrier package, transmission control protocol
TF	trap flag
TFT	thin-film transistor
TIA	Telecommunications Information Administration
TPE	twisted pair ethernet
TPI	track per inch
TTL	transistor-transistor logic
TV	television
TX	transmit
UART	universal asynchronous receiver/transmitter
UDMA	Ultra DMA
URL	Uniform resource locator
us/µs	microsecond
USB	Universal Serial Bus
UTP	unshielded twisted pair
V	volt

Table 1-1 *(Continued)*
Acronyms and Abbreviations

Acronym or Abbreviation	Description
VAC	Volts alternating current
VDC	Volts direct current
VESA	Video Electronic Standards Association
VGA	video graphics adapter
VLSI	very large scale integration
VRAM	Video RAM
W	watt
WOL	Wake-On-LAN
WRAM	Windows RAM
ZF	zero flag
ZIF	zero insertion force (socket)

2

System Overview

2.1 Introduction

The HP Compaq dc7800 Business PC personal computers (Figure 2-1) deliver an outstanding combination of manageability, serviceability, and compatibility for enterprise environments. Based on the Intel processor with the Intel Q35 Express chipset, these systems emphasize performance along with industry compatibility. These models feature a similar architecture incorporating both PCI 2.3 and PCIe buses. All models are easily upgradeable and expandable to keep pace with the needs of the office enterprise.

Figure 2-1. HP Comapq dc7800 Business PCs

This chapter includes the following topics:

- Features (2.2)
- System architecture (2.3)
- Specifications (2.4)

2.2 Features

The following standard features are included on all models unless otherwise indicated:

- Intel processor in LGA775 (Socket T) package
- Integrated graphics controller
- PC2-6400 and PC2-5300 (DDR2) DIMM support
- Hard drive fault prediction
- Eight USB 2.0-compliant ports
- High definition (HD) audio processor with one headphone output, at least one microphone input, one line output, and one line input
- Network interface controller providing 10/100/1000Base T support
- Plug 'n Play compatible (with ESCD support)
- Intelligent Manageability support
- Intel vPro Technology using Active Management Technology (AMT) 3.0 on select models
- Security features including:
  - Flash ROM Boot Block
  - Diskette drive disable, boot disable, write protect
  - Power-on password
  - Administrator password
  - Serial/parallel port disable (SFF and CMT form factors only)
  - Hood (cover) sense
  - Hoodlock (SFF and CMT form factors only)
  - USB port disable
- PS/2 enhanced keyboard
- PS/2 optical scroll mouse
- Energy Star 4.0 with 80 Plus compliancy standard on USDT form factors (option available on SFF and CMT form factors)

Table 2-1 shows the differences in features between the different PC series based on form factor:

Table 2-1
Feature Difference Matrix by Form Factor

	USDT	SFF	CMT
Memory:			
# & type of sockets	2 SODIMM	4 DIMM	4 DIMM
Maximum memory	4GB	8GB	8GB
Serial ports	0	1 std., 1 opt. [1]	1 std., 1 opt. [1]
Parallel ports	0	1	1
DVI-D graphics port	1	0	0
Drive bays:			
Externally accessible	1	2	4
Internal	1	1	2
PCIe slots:			
x16 graphics	0	1 [3] [4]	1 [5]
x1	1 [2]	2 [3]	2
PCI 2.3 32-bit 5-V slots	0	1 half-height or 2 full-height [6]	3 full-height
Power Supply Unit:			
Module type	external	internal	internal
Power rating	135-watt	240-watt	365-watt

NOTES:

[1] 2nd serial port requires optional cable/bracket assembly.

[2] PCIe Mini Card slot.

[3] Supports low-profile card in standard configuration. Not accessible if PCI riser card field option is installed.

[4] Accepts low-profile, reversed-layout ADD2/SDVO PCIe card: height = 2.5 in., length = 6.6 in.

[5] Accepts reversed layout ADD2/SDVO card: height = 4.2 in., length = 10.5 in.

[6] Full-height PCI slots require installation of PCI riser card field option (full-height dimensions: height = 4.2 in., length = 6.875 in).

2.3 System Architecture

The systems covered in this guide feature an architecture based on the Intel Q35 Express chipset (Figure 2-13). All systems covered in this guide include the following key components:

- Intel Pentium Dual-Core, Core 2 Duo, Core 2 Quad, or Celeron processor.
- Intel Q35 Express chipset - Includes Q35 GMCH north bridge and 82801 ICH9-DO south bridge
- SMC SCH5327 super I/O controller supporting PS/2 keyboard and mouse peripherals
- AD1884 audio controller supporting line in, line out, microphone in, and headphones out
- Intel 82566DM 10/100/1000 network interface controller

The Q35 chipset provides a major portion of system functionality. Designed to compliment the latest Intel processors, the Q35 GMCH integrates with the processor through a 800/1066/1333-MHz Front-Side Bus (FSB) and communicates with the ICH9-DO component through the Direct Media Interface (DMI). The integrated graphics controller of the Q35 on SFF and CMT systems can be upgraded through a PCI Express (PCIe) x16 graphics slot. All systems include a serial ATA (SATA) hard drive in the standard configuration. The USDT model supports a Slimline Optical Drive through a legacy parallel ATA 100 interface.

Table 2-2 lists the differences between models by form factor.

Table 2-2.
Architectural Differences By Form Factor

Function	USDT	SFF	CMT
Memory sockets	2 SODIMMs	4 DIMMs	4 DIMMs
PCIe x16 graphics slot?	No	Yes [1]	Yes
# of PCIe x1 slots	1 [2]	2 [1]	2
# of PCI 2.3 slots	0	1 [3]	3
Serial / parallel ports	0	1 [4]	1 [4]
Parallel ports	0	1	1
SATA interfaces	1	3	4

Notes:

[1] Low-profile slot. Not accessible if PCI riser is installed.
[2] PCIe Mini-Card slot.
[3] Low-profile slot in standard configuration. 2 full-height slots supported with optional PCI riser.
[4] 2nd serial port possible with optional adapter.

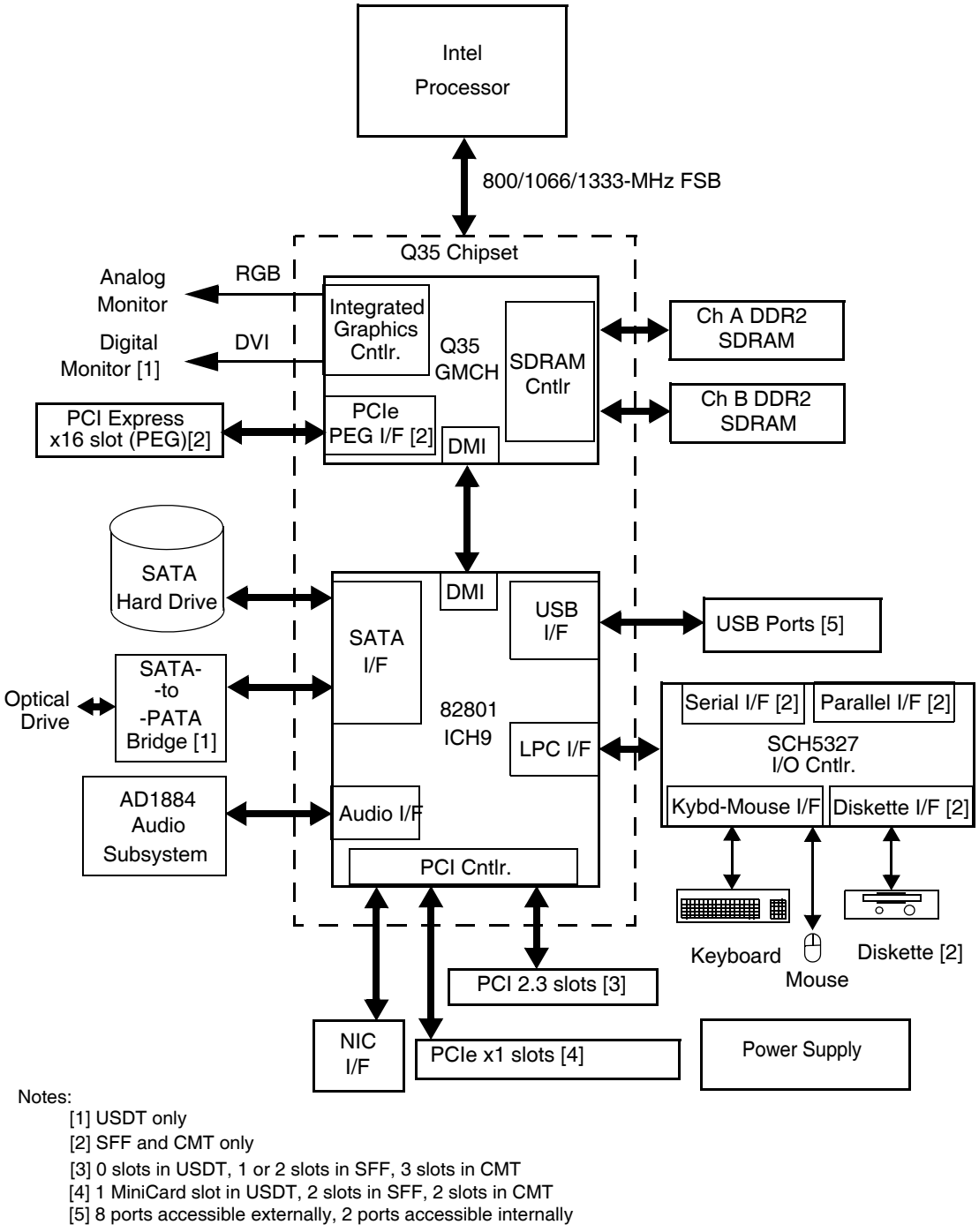


Figure 2-2. HP Comapq dc7800 Business PC Architecture, Block diagram

2.3.1 Intel Processor Support

The models covered in this guide are designed to support the following processor types:

- Intel Celeron: energy-efficient single-core performance
- Intel Pentium Dual-Core: Dual core performance
- Intel Core2 Duo: energy-efficient dual-core performance
- Intel Core2 Quad: energy efficient quad-core design

These processors are backward-compatible with software written for earlier x86 microprocessors and include streaming SIMD extensions (SSE, SSE2, and SSE3) for enhancing 3D graphics and speech processing performance.

The system board includes a zero-insertion-force (ZIF) Socket-T designed for mounting an LGA775-type processor package.

CAUTION: The USDT form factor can support a processor rated up to 65 watts. The SFF and CMT form factors can support a processor rated up to 95 watts. Exceeding these limits can result in system damage and lost data.

The processor heatsink/fan assembly mounting differs between form factors. Always use the same assembly or one of the same type when replacing the processor. Refer to the applicable Service Reference Guide for detailed removal and replacement procedures of the heatsink/fan assembly and the processor.

2.3.2 Chipset

The Intel Q35 Express chipset consists of a Graphics Memory Controller Hub (GMCH) and an enhanced I/O controller hub (ICH9-DO). Table 2-3 compares the functions provided by the chipsets.

Table 2-3
Chipset Components and Functionality

Components	Function
Q35 GMCH	Intel Graphics Media Accelerator 3100 (integrated graphics controller) PCIe x16 graphics interface (SFF and CMT only) SDRAM controller supporting unbuffered, non-ECC PC2-6400 DDR2 DIMMs or SODIMMs 800-, 1066-, or 1333-MHz FSB
82801 ICH9-DO	PCI 2.3 bus I/F PCI Express x1 LPC bus I/F SMBus I/F SATA I/F HD audio interface RTC/CMOS IRQ controller Power management logic USB 1.1/2.0 controllers supporting 12 ports (these systems provide 8 external, 2 internal) Gigabit Ethernet controller

The I/O controller hub (ICH9-DO) features Intel vPro, which includes Active Management Technology (AMT). AMT is a hardware/firmware solution that operates on auxiliary power to allow 24/7 support of network alerting and management of the unit without regard to the power state or operating system. AMT capabilities include:

- System asset recovery (hardware and software configuration data)
- OS-independent system wellness and healing
- Software (virus) protection/management

2.3.3 Support Components

Input/output functions not provided by the chipset are handled by other support components. Some of these components also provide “housekeeping” and various other functions as well. Table 2-4 shows the functions provided by the support components.

Table 2-4
Support Component Functions

Component Name	Function
SCH5327 I/O Controller	Keyboard and pointing device I/F Diskette I/F [1] Serial I/F (COM1and COM2) [1] Parallel I/F (LPT1, LPT2, or LPT3) [1] PCI reset generation Interrupt (IRQ) serializer Power button and front panel LED logic GPIO ports Processor over temperature monitoring Fan control and monitoring Power supply voltage monitoring SMBus and Low Pin Count (LPC) bus I/F
Intel 82566DM Network Interface Controller	10/100/1000 Fast Ethernet network interface controller.
AD1884 HD Audio Codec	Audio mixer Two digital-to-analog 2-channel converters Two analog-to-digital 2-channel converters Analog I/O Supports two 2-channel (stereo) audio streams

NOTE:
[1] Not used in USDT form factor.

2.3.4 System Memory

These systems implement a dual-channel Double Data Rate (DDR2) memory architecture. All models support DDR2 800- and 667-MHz DIMMs.

DDR and DDR2 DIMMs are NOT interchangeable.

The USDT system provides two SODIMM sockets supporting up to four gigabytes of memory while the SFF and CMT form factors provide four DIMM sockets and support a total of eight gigabytes of memory.

SODIMM and DIMM components are NOT interchangeable.

2.3.5 Mass Storage

All models support at least two mass storage devices, with one being externally accessible for removable media. These systems provide the following interfaces for internal storage devices:

USDT: one SATA interface, one SATA-to-PATA bridge/interface for a Slimline optical drive

SFF: three SATA interfaces

CMT: four SATA interfaces

These systems may be preconfigured or upgraded with a SATA hard drive and one removable media drive such as a CD-ROM drive.

2.3.6 Serial and Parallel Interfaces

The SFF and CMT form factors include a serial port and a parallel port, both of which are accessible at the rear of the chassis. The SFF and CMT form factors may be upgraded with a second serial port option.

The serial interface is RS-232-C/16550-compatible and supports standard baud rates up to 115,200 as well as two high-speed baud rates of 230K and 460K. The parallel interface is Enhanced Parallel Port (EPP1.9) and Enhanced Capability Port (ECP) compatible, and supports bi-directional data transfers.

2.3.7 Universal Serial Bus Interface

All models provide ten Universal Serial Bus (USB) ports. Two ports are accessible at the front of the unit, six ports are accessible on the rear panel, and two ports are accessible on the system board. The SFF and CMT form factors support a media card reader module that connects to the two internal ports. These systems support USB 1.1 and 2.0 functionality on all ports.

2.3.8 Network Interface Controller

All models feature an Intel gigabit Network Interface Controller (NIC) integrated on the system board. The controller provides automatic selection of 10BASE-T, 100BASE-TX, or 1000BASE-T operation with a local area network and includes power-down, wake-up, Alert-On-LAN (AOL), Alert Standard Format (ASF), and Active Management Technology (AMT) features. An RJ-45 connector with status LEDs is provided on the rear panel.

2.3.9 Graphics Subsystem

These systems use the Q35 GMCH component, which includes an integrated graphics controller that can drive an external VGA monitor. The controller implements Dynamic Video Memory Technology (DVMT 3.0) for video memory. Table 2-5 lists the key features of the integrated graphics subsystem.

Table 2-5
Integrated Graphics Subsystem Statistics

	Q35 GMCH Integrated Graphics Controller
Recommended for	Hi 2D, Entry 3D
Bus Type	Int. PCI Express
Memory Amount	8 MB pre-allocated
Memory Type	DVMT 3.0
DAC Speed	400 MHz
Maximum 2D Resolution	2048x1536 @ 85 Hz
Software Compatibility	Quick Draw, DirectX 9.0, Direct Draw, Direct Show, Open GL 1.4, MPEG 1-2, Indeo
Outputs	1 RGB

The IGC supports dual independent display for expanding the desktop viewing area across two monitors. The USDT form factor includes a DVI-D interface for direct connection with a digital video monitor. The graphics subsystem of the SFF and CMT systems can be upgraded by installing an SDVO ADD2 card or PCIe x16 graphics card in the PCIe x16 graphics slot.

2.3.10 Audio Subsystem

These systems use the integrated High Definitions audio controller of the chipset and the ADI AD1884 High Definition audio codec. HD audio provides improvements over AC'97 audio such as higher sampling rates, refined signal interfaces, and audio processors with a higher signal-to-noise ratio. The audio line input jack can be re-configured as a microphone input, and multi-streaming is supported. These systems include a 1.5-watt output amplifier driving an internal speaker. All models include front panel-accessible stereo microphone in and headphone out audio jacks.

2.4 Specifications

This section includes the environmental, electrical, and physical specifications for the systems covered in this guide. Where provided, metric statistics are given in parenthesis. Specifications are subject to change without notice.

Table 2-6
Environmental Specifications (Factory Configuration)

Parameter	Operating	Non-operating
Ambient Air Temperature	50° to 95° F (10° to 35° C, max. rate of change ≤ 10°C/Hr)	-22° to 140° F (-30° to 60° C, max. rate of change ≤ 20°C/Hr)
Shock (w/o damage)	5 Gs [1]	20 Gs [1]
Vibration	0.000215 G^2/Hz, 10-300 Hz	0.0005 G^2/Hz, 10-500 Hz
Humidity	10-90% Rh @ 28° C max. wet bulb temperature	5-95% Rh @ 38.7° C max. wet bulb temperature
Maximum Altitude	10,000 ft (3048 m) [2]	30,000 ft (9144 m) [2]

NOTE:
[1] Peak input acceleration during an 11 ms half-sine shock pulse.
[2] Maximum rate of change: 1500 ft/min.

Table 2-7
Power Supply Electrical Specifications

Parameter	Value
Input Line Voltage:	
Nominal:	100–240 VAC
Maximum	90–264 VAC
Input Line Frequency Range:	
Nominal	50–60 Hz
Maximum	47–63 Hz
Energy Star 4.0 with 80 Plus compliancy	
USDT	Standard
SFF & CMT	Optional
Maximum Continuous Power:	
USDT	135 watts
SFF	240 watts
CMT	365 watts

NOTE:
Energy Star 4.0 with 80 Plus compliancy option available for SFF and CMT form factors.

Table 2-8
Physical Specifications

Parameter	USDT [2]	SFF [2]	CMT [3]
Height	2.60 in (6.60 cm)	3.95 in (10.03 cm)	17.63 in (44.8 cm)
Width	9.90 in (25.15 cm)	13.3 in (33.78 cm)	7.0 in (16.8 cm)
Depth	10.0 in (25.40 cm)	14.9 in (37.85 cm)	17.8 in (45.21 cm)
Weight [1]	7.0 lb (3.18 kg)	18.75 lb (8.50 kg)	26.2 lb (11.89 kg)
Load-bearing ability of chassis [4]	77.1 lb (35 kg)	77.1 lb (35 kg)	77.1 lb (35 kg)

NOTES:

[1] System configured with 1 hard drive, 1 diskette drive (SFF and CMT only), and no PCI cards.

[2] Desktop (horizontal) configuration.

[3] Minitower configuration. For desktop configuration, swap Height and Width dimensions.

[4] Applicable to unit in desktop orientation only and assumes reasonable type of load such as a monitor.

Table 2-9
Diskette Drive Specifications

Parameter	Measurement
Media Type	3.5 in 1.44 MB/720 KB diskette
Height	1/3 bay (1 in)
Bytes per Sector	512
Sectors per Track:	
High Density	18
Low Density	9
Tracks per Side:	
High Density	80
Low Density	80
Read/Write Heads	2
Average Access Time:	
Track-to-Track (high/low)	3 ms/6 ms
Average (high/low)	94 ms/169 ms
Settling Time	15 ms
Latency Average	100 ms

Table 2-10
Optical Drive Specifications

Parameter	DVD-ROM	CD-RW/DVD-ROM Combo	DVD/CD-RW SuperMulti LightScribe Combo
Interface Type	SATA [1]	SATA [1]	SATA [1]
Max. read/write speeds by media type	DVD-RAM: 4x/na DVD+RW: 8x/na DVD-RW: 8x/na DVD+R DL: 8x/na DVD-R DL: 8x/na DVD-ROM: 16x/na DVD+R: 8x/na DVD-R: 8x/na CD-ROM: 48x/na CD-RW: 32x/na CD-R: 48x/na	DVD-RAM: 12x/12x DVD+RW: 8x/8x DVD-RW: 8x/6x DVD+R DL: 8x/8x DVD-R DL: 8x/8x DVD-ROM: 16x/na DVD-ROM DL: 8x/na DVD+R: 16x/16x DVD-R: 16x/16x CD-ROM: 48x/na CD-RW: 32x/32x CD-R: 48x/48x	DVD-RAM: 12x/12x DVD+RW: 8x/8x DVD-RW: 8x/6x DVD+R DL: 8x/8x DVD-R DL: 8x/8x DVD-ROM: 16x/na DVD-ROM DL: 8x/na DVD+R: 16x/16x DVD-R: 16x/16x CD-ROM: 48x/na CD-RW: 32x/32x CD-R: 48x/48x
Maximum Transfer Rate (Reads)	DVD:, 21.6 KB/s; CD: 7.2 KB/s	DVD:, 21.6 KB/s; CD: 7.2 KB/s	DVD:, 21.6 KB/s; CD: 7.2 KB/s
Media Capacity (DVD)	DL: 8.5 GB, Std: 4.7 GB	DL: 8.5 GB, Std: 4.7 GB	DL: 8.5 GB, Std: 4.7 GB
Average Access Time:			
Random	DVD: <140 ms, CD: <125 ms	DVD: <140 ms, CD: <125 ms	DVD: <140 ms, CD: <125 ms
Full Stroke	DVD: <250 ms, CD: <210 ms	DVD: <250 ms, CD: <210 ms	DVD: <250 ms, CD: <210 ms
Media lable creation?	No	No	Yes [2]

NOTE
[1] USDT models use “slim” drive that uses an IDE interface through SATA bridge.
[2] Requires special label-etchable media.

Table 2-11
Hard Drive Specifications

Parameter	80 GB	160 GB	250 GB [4]
Drive Size	2.5 & 3.5 in.[1]	2.5 & 3.5 in [1]	3.5 in
Interface	SATA	SATA	SATA
Transfer Rate	1.5 & 3.0 Gb/s [2]	1.5 & 3.0 Gb/s [2]	3.0 Gb/s
Drive Protection System Support?	Yes	Yes	Yes
Typical Seek Time (w/settling)			
Single Track	0.8 ms	0.8 ms	1.0 ms
Average	9 ms	9 ms	11 ms
Full Stroke	17 ms	17 ms	18 ms
Disk Format (logical blocks)	156,301,488	320,173,056	488,397,168
Rotation Speed	5400/7200/ 10K RPM [3]	5400/7200/ 10K RPM [3]	7200 RPM
Drive Fault Prediction	SMART IV	SMART IV	SMART IV

NOTES:

[1] USDT supports 2.5-in. drives only.

[2] USDT supports 1.5 Gb/s drives only.

[3] USDT supports up to 7200-RPM drives only.

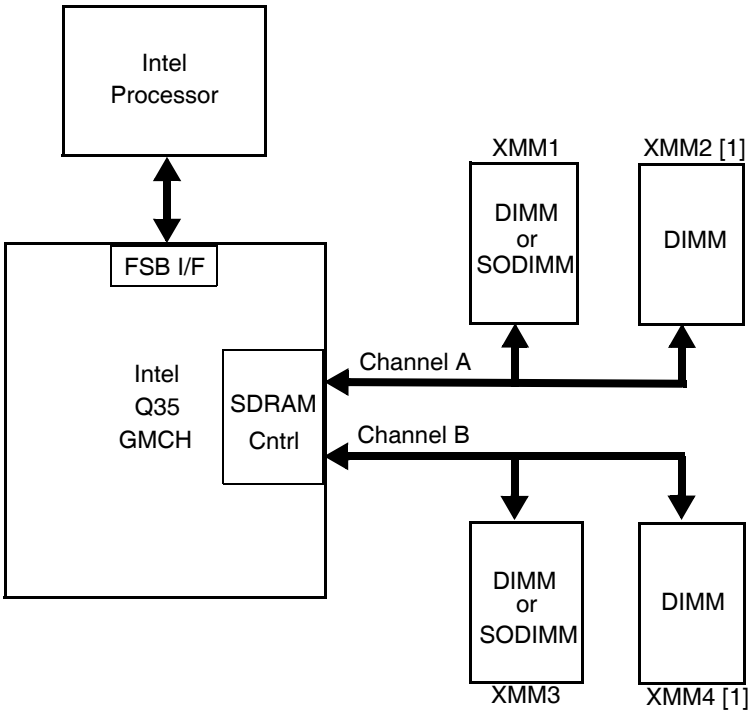
[4] Supported by SFF and CMT form factors only.

3

Processor/Memory Subsystem

3.1 Introduction

This chapter describes the processor/memory subsystem. These systems support the Intel Pentium and Core processor families and use the Q35 chipset (Figure 3-1). These systems support PC2-6400 and PC2-5300 DDR2 memory modules.



Note:
[1] Not present on USDT form factor.

Figure 3-1. Processor/Memory Subsystem Architecture

This chapter includes the following topics:

- Intel Pentium processor (3.2)
- Memory subsystem (3.3)

3.2 Intel Processors

These systems each feature an Intel processor in a FC-LGA775 package mounted with a heat sink in a zero-insertion force socket. The mounting socket allows the processor to be easily changed for upgrading.

3.2.1 Intel Processor Overview

The models covered in this guide support Intel Celeron, Pentium, and Core 2 processors, including the latest Intel Core 2 Duo, and Core 2 Quad processors.

Key features of supported Intel processors include:

- Dual- or quad-core architecture—Provides full parallel processing.
- Hyper-Threading Technology—Featured in some Intel Pentium and Core Processors, the main processing loop has twice the depth (20 stages) of earlier processors allowing for increased processing frequencies.
- Execution Trace Cache— A new feature supporting the branch prediction mechanism, the trace cache stores translated sequences of branching micro-operations (ops) and is checked when suspected re-occurring branches are detected in the main processing loop. This feature allows instruction decoding to be removed from the main processing loop.
- Rapid Execution Engine—Arithmetic Logic Units (ALUs) run at twice (2x) processing frequency for higher throughput and reduced latency.
- Up to 8-MB of L2 cache—Using a 32-byte-wide interface at processing speed, the large L2 cache provides a substantial increase.
- Advanced dynamic execution—Using a larger (4K) branch target buffer and improved prediction algorithm, branch mis-predictions are significantly reduced
- Additional Streaming SIMD extensions (SSE2 andSSE3)—In addition to the SSE support provided by previous Pentium processors, the Pentium 4 processor includes an additional 144 MMX instructions, further enhancing:
  - Streaming video/audio processing
  - Photo/video editing
  - Speech recognition
  - 3D processing
  - Encryption processing
- Quad-pumped Front Side Bus (FSB)—The FSB uses a 200-MHz clock for qualifying the buses' control signals. However, address information is transferred using a 2x strobe while data is transferred with a 4x strobe, providing a maximum data transfer rate that is four times that of earlier processors.

The Intel processor increases processing speed by using higher clock speeds with hyper-pipelined technology, therefore handling significantly more instructions at a time. The Arithmetic Logic Units (ALUs) of all processors listed above run at twice the core speed.

3.2.2 Processor Changing/Upgrading

All models use the LGA775 ZIF (Socket T) mounting socket. These systems require that the processor use an integrated heatsink/fan assembly. A replacement processor must use the same type heatsink/fan assembly as the original to ensure proper cooling. The heatsink and attachment clip are specially designed provide maximum heat transfer from the processor component.

CAUTION: Attachment of the heatsink to the processor is critical on these systems. Improper attachment of the heatsink will likely result in a thermal condition. Although the system is designed to detect thermal conditions and automatically shut down, such a condition could still result in damage to the processor component. Refer to the applicable Service Reference Guide for processor installation instructions.

These sysems are available with one of the following processors listed in Table 3-1.

Table 3-1
Supported Processors

Intel Model	Core design	Features	Clock Speed in GHz	FSB Speed in MHz	L2 Cache	Form Factor support
Q6700	quad	VT, [1]	2.66	1066	8 MB	SFF, CMT
Q6600	quad	VT, [1]	2.40	1066	8 MB	SFF, CMT
E6850	dual	vPro, VT, TXT, [1]	3.00	1333	4 MB	all
E6750	dual	vPro, VT, TXT, [1]	2.66	1333	4 MB	all
E6550	dual	vPro, VT, TXT, [1]	2.33	1333	4 MB	all
E4500	dual	[1]	2.20	800	2 MB	all
E4400	dual	[1]	2.00	800	2 MB	all
E2180	dual	[1]	2.00	800	1 MB	all
E2160	dual	[1]	1.80	800	1 MB	all
440	single	[1]	2.00	800	512 KB	all

NOTE:
[1] Standard Intel feature set including EM64T, XD, and EIST support. Refer to www.Intel.com for detailed information.

CAUTION: The USDT form factor can support a processor with a maximum power consumption of 65 watts. The SFF and CMT form factors can support a processor with a maximum power consumption of 95 watts. Exceeding these limits can result in system damage and lost data.

3.3 Memory Subsystem

All models support non-ECC PC2-5300 and PC2-6400 DDR2 memory. The USDT form factor supports up to four gigabytes of memory while the SFF and CMT form factors support up to eight gigabytes of memory.

The DDR SDRAM "PCxxxx" reference designates bus bandwidth (i.e., a PC2-5300 module can, operating at a 667-MHz effective speed, provide a throughput of 5300 MBps (8 bytes × 667MHz)). Memory speed types may be mixed within a system, although the system BIOS will set the memory controller to work at speed of the slowest memory module.

The USDT system board provides two SODIMM sockets and the SFF and CMT system boards provide four DIMM sockets

- XMM1, channel A (black)
- XMM2, channel A (white, not present in USDT form factor)
- XMM3, channel B (white)
- XMM4, channel B (white, not present in USDT form factor)

Memory modules do not need to be installed in pairs although installation of pairs (especially matched sets) provides the best performance. The XMM1 socket must be populated for proper support of Intel Advanced Management Technology (AMT). The BIOS will detect the module population and set the system accordingly as follows:

- Single-channel mode - memory installed for one channel only
- Dual-channel asymetric mode - memory installed for both channels but of unequal channel capacities.
- Dual-channel interleaved mode (recommended) - memory installed for both channels and offering equal channel capacities, proving the highest performance.

These systems support memory modules with the following parameters:

- Unbuffered, compatible with SPD rev. 1.0
- 512-Mb, and 1-Gb memory technologies for x8 and x16 devices
- CAS latency (CL) of 5 or 6 (depending on memory speed)
- Single or double-sided
- Non-ECC memory only

The SPD format supported by these systems complies with the JEDEC specification for 128-byte EEPROMs. This system also provides support for 256-byte EEPROMs to include additional HP-added features such as part number and serial number.

If BIOS detects an unsupported memory module, a "**memory incompatible**" message will be displayed and the system will halt. **These systems are shipped with non-ECC modules only**.

An installed mix of memory module types is acceptable but operation will be constrained to the level of the module with the lowest (slowest) performance.

If an incompatible memory module is detected the NUM LOCK will blink for a short period of time during POST and an error message may or may not be displayed before the system hangs.

3.3.1 Memory Upgrading

Table 3-2 shows suggested memory configurations for these systems. Note that the USDT form factor provides only two memory sockets.

Table 3-2 does not list all possible configurations.

Table 3-2.
Memory Socket Loading [1]

Channel A		Channel B		
Socket 1	**Socket 2 [2]**	**Socket 3**	**Socket 4 [2]**	**Total**
512 MB	none	none	none	512-MB
512 MB	none	512 MB	none	1-GB (dual-channel symetrical)
1-GB	none	none	none	1-GB
1 GB	none	1 GB	none	2 GB (dual-channel symetrical)
1 GB	1 GB	1 GB	1 GB	4-GB (dual-channel symetrical)
2 GB	none	2 GB	none	4-GB (dual-channel symetrical)
2 GB	2-GB	2 GB	2 GB	8-GB (dual-channel symetrical)

NOTE:

[1] USDT form factor uses SODIMM sockets. SFF and CMT form factors use DIMM sockets.

[2] Not present on USDT form factor.

HP recommends using symmetrical loading (same-capacity, same-speed modules across both channels) to achieve the best performance.

CAUTION: Always power down the system and disconnect the power cord from the AC outlet before adding or replacing memory modules. Changing memory modules while the unit is plugged into an active AC outlet could result in equipment damage.

Memory amounts over 3 GB may not be fully accessible with 32-bit operating systems due to system resource requirements. Addressing memory above 4 GB requires a 64-bit operating system.

3.3.2 Memory Mapping and Pre-allocation

Figure 3-2 shows the system memory map. The Q35 Express chipset includes a Management Engine that pre-allocates a portion of system memory (16 MB for one module, 32 MB for two modules) for managment functions. In addition, the internal graphics controller pre-allocates a portion of system memory for video use (refer to chapter 6). Pre-allocated memory is not available to the operating system. The amount of system memory reported by the OS will be the total amount installed less the pre-allocated amount.

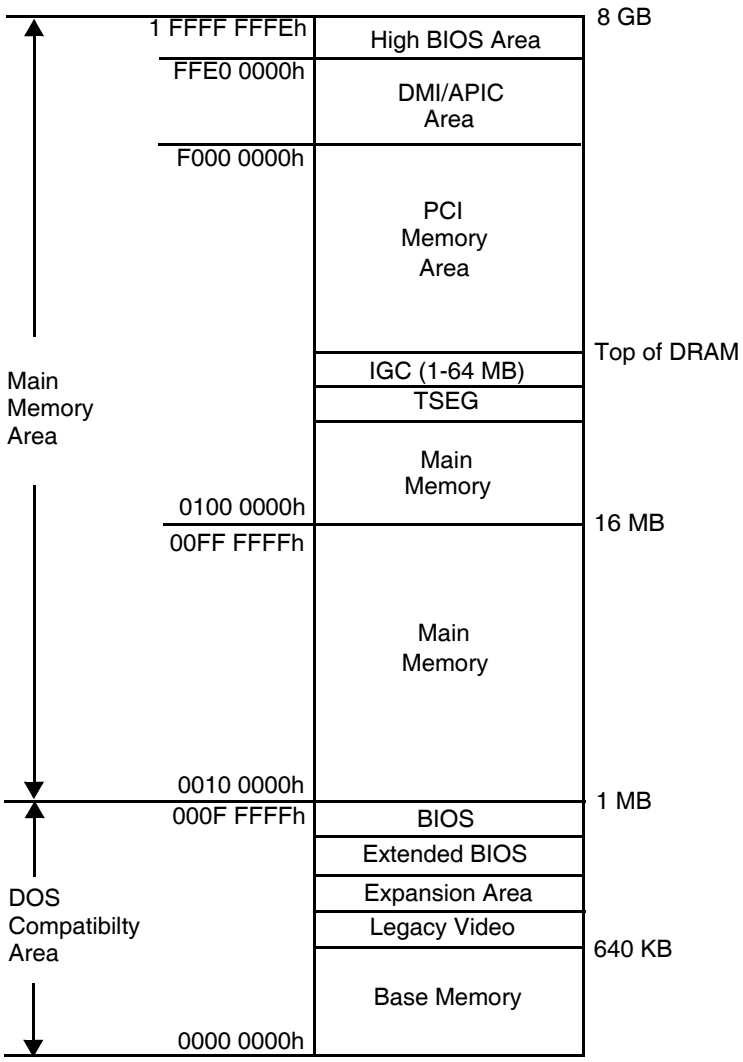


Figure 3-2. System Memory Map (for maximum of 8 gigabytes)

All locations in memory are cacheable. Base memory is always mapped to DRAM. The next 128 KB fixed memory area can, through the north bridge, be mapped to DRAM or to PCI space. Graphics RAM area is mapped to PCI locations.

4

System Support

4.1 Introduction

This chapter covers subjects dealing with basic system architecture and covers the following topics:

- PCI bus overview (4.2)
- System resources (4.3)
- Real-time clock and configuration memory (4.4)
- System management (4.5)
- Register map and miscellaneous functions (4.6)

This chapter covers functions provided by off-the-shelf chipsets and therefore describes only basic aspects of these functions as well as information unique to the systems covered in this guide. For detailed information on specific components, refer to the applicable manufacturer's documentation.

4.2 PCI Bus Overview

This section describes the PCI bus in general and highlights bus implementation for systems covered in this guide. For detailed information regarding PCI bus operation, refer to the appropriate PCI specification or the PCI web site: www.pcisig.com.

These systems implement the following types of PCI buses:

- PCI 2.3 - Legacy parallel interface operating at 33-MHz
- PCI Express - High-performance interface capable of using multiple TX/RX high-speed lanes of serial data streams

4.2.1 PCI 2.3 Bus Operation

The PCI 2.3 bus consists of a 32-bit path (AD31-00 lines) that uses a multiplexed scheme for handling both address and data transfers. A bus transaction consists of an address cycle and one or more data cycles, with each cycle requiring a clock (PCICLK) cycle. High performance is achieved during burst modes in which a transaction with contiguous memory locations requires that only one address cycle be conducted and subsequent data cycles are completed using auto-incremented addressing.

Devices on the PCI bus must comply with PCI protocol that allows configuration of that device by software. In this system, configuration mechanism #1 (as described in the PCI Local Bus specification Rev. 2.3) is employed.

Table 4-1 shows the standard configuration of device numbers and IDSEL connections for components and slots residing on a PCI 2.3 bus.

Table 4-1
PCI Component Configuration Access

PCI Component	Notes	Function #	Device #	PCI Bus #	IDSEL Wired to:
Q35 GMCH:					--
Host/DMI Bridge		0	28	0	
Host/PCI Expr. Bridge		0	1	0	
Integrated Graphics Cntlr.		0	2	0	
PCI Express x16 graphics slot		0	0	1	--
82801EB ICH9					--
PCI Bridge		0	30	0	
LPC Bridge		0	31	0	
Serial ATA Controller #1		2	31	0	
SMBus Controller		3	31	0	
Serial ATA Controller #2	[1]	5	31	0	
Thermal System		6	31	0	
USB 1.1 Controller #1		0	29	0	
USB 1.1 Controller #2		1	29	0	
USB 1.1 Controller #3		2	29	0	
USB 1.1 Controller #4		3 [2]	29 [2]	0	
USB 1.1 Controller #5		1	26	0	
USB 2.0 Controller #1		7	29	0	
USB 2.0 Controller #2		7	26	0	
Network Interface Controller		0	25	0	
Intel HD audio controller		0	27	0	
PCIe port 1		0	28	0	
PCIe port 2	[3]	1	28	0	
PCIe port 3	[1]	2	28	0	
PCIe port 4	[1]	3	28	0	
PCIe port 5	[1]	4	28	0	
PCIe port 6		5	28	0	
PCI 2.3 slot 1	[3]	0	4	7	AD20
PCI 2.3 slot 2	[3]	0	11	7	AD25
PCI 2.3 slot 3	[4]	0	10	7	AD27
PCIe x1 slot 1	[3]	0	0	32	
PCIe x1 slot 2	[3]	0	0	48	

NOTES:

[1] Function not used in these systems.

[2] Mapping for USB 1.1 Controller #4 if USB ports 9 and 10 and USB 2.0 Controller #2 are disabled. Otherwise, mapping for USB 1.1 controller #4 is F0:D25.

[3] SFF and CMT form factors only.

[4] CMT form factor only

The PCI bus supports a bus master/target arbitration scheme. A bus master is a device that has been granted control of the bus for the purpose of initiating a transaction. A target is a device that is the recipient of a transaction. The Request (REQ), Grant (GNT), and FRAME signals are used by PCI bus masters for gaining access to the PCI bus. When a PCI device needs access to the PCI bus (and does not already own it), the PCI device asserts its REQn signal to the PCI bus arbiter (a function of the system controller component). If the bus is available, the arbiter asserts the GNTn signal to the requesting device, which then asserts FRAME and conducts the address phase of the transaction with a target. If the PCI device already owns the bus, a request is not needed and the device can simply assert FRAME and conduct the transaction. Table 4-2 shows the grant and request signals assignments for the devices on the PCI bus.

Table 4-2.
PCI Bus Mastering Devices

Device	REQ/GNT Line	Note
PCI Connector Slot 1	REQ0/GNT0	[1]
PCI Connector Slot 2	REQ1/GNT1	[1]
PCI Connector Slot 3	REQ2/GNT2	[2]

NOTE:

[1] SFF and CMT form factors only.

[2] CMT form factor only

PCI bus arbitration is based on a round-robin scheme that complies with the fairness algorithm specified by the PCI specification. The bus parking policy allows for the current PCI bus owner (excepting the PCI/ISA bridge) to maintain ownership of the bus as long as no request is asserted by another agent. Note that most CPU-to-DRAM accesses can occur concurrently with PCI traffic, therefore reducing the need for the Host/PCI bridge to compete for PCI bus ownership.

4.2.2 PCI Express Bus Operation

The PCI Express (PCIe) bus is a high-performace extension of the legacy PCI bus specification. The PCI Express bus uses the following layers:

- Software/driver layer
- Transaction protocol layer
- Link layer
- Physical layer

Software/Driver Layer

The PCI Express bus maintains software compatibility with PCI 2.3 and earlier versions so that there is no impact on existing operating systems and drivers. During system intialization, the PCI Express bus uses the same methods of device discovery and resource allocation that legacy PCI-based operating systems and drivers are designed to use.

Transaction Protocol Layer

The transaction protocol layer processes read and write requests from the software/driver layer and generates request packets for the link layer. Each packet includes an identifier allowing any required responcse packets to be directed to the originator.

Link Layer

The link layer provides data integrity by adding a sequence information prefix and a CRC suffix to the packet created by the transaction layer. Flow-control methods ensure that a packet will only be transferred if the receiving device is ready to accomodate it. A corrupted packet will be automatically re-sent.

Physical Layer

The PCI Express bus uses a point-to-point, high-speed TX/RX serial lane topology. One or more full-duplex lanes transfer data serially, and the design allows for scalability depending on end-point capabilities. Each lane consists of two differential pairs of signal paths; one for transmit, one for receive (Figure 4-1).

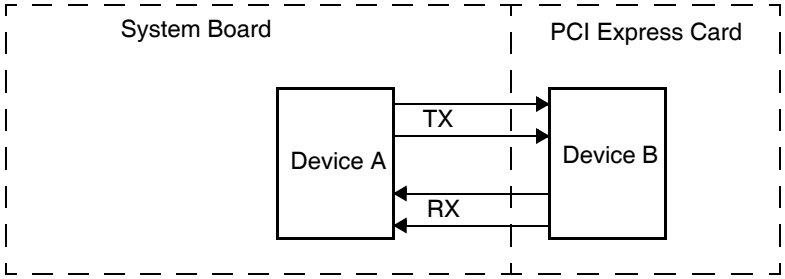


Figure 4-1. PCI Express Bus Lane

Each byte is transferred using 8b/10b encoding. which embeds the clock signal with the data. Operating at a 2.5 Gigabit transfer rate, a single lane can provide a data flow of 200 MBps. The bandwidth is increased if additional lanes are available for use. During the initialization process, two PCI Express devices will negotiate for the number of lanes available and the speed the link can operate at. In a x1 (single lane) interface, all data bytes are transferred serially over the lane. In a multi-lane interface, data bytes are distributed across the lanes using a multiplex scheme.

4.2.3 Option ROM Mapping

During POST, the PCI bus is scanned for devices that contain their own specific firmware in ROM. Such option ROM data, if detected, is loaded into system memory's DOS compatibility area (refer to the system memory map shown in chapter 3).

4.2.4 PCI Interrupts

Eight interrupt signals (INTA- thru INTH-) are available for use by PCI devices. These signals may be generated by on-board PCI devices or by devices installed in the PCI slots. For more information on interrupts including PCI interrupt mapping refer to the “System Resources” section 4.3.

4.2.5 PCI Power Management Support

This system complies with the PCI Power Management Interface Specification (rev 1.0). The PCI Power Management Enable (PME-) signal is supported by the chipset and allows compliant PCI peripherals to initiate the power management routine.

4.2.6 PCI Connectors

PCI 2.3 Connector

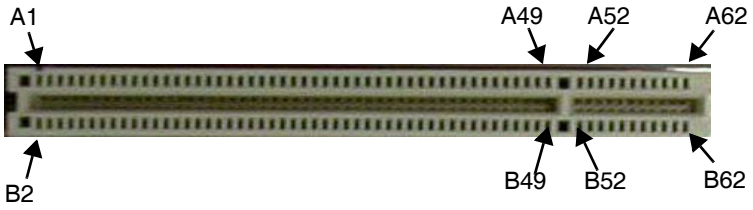


Figure 4-2. 32-bit, 5.0-volt PCI 2.3 Bus Connector

Table 4-3.
PCI 2.3 Bus Connector Pinout

Pin	B Signal	A Signal	Pin	B Signal	A Signal	Pin	B Signal	A Signal
01	-12 VDC	TRST-	22	GND	AD28	43	+3.3 VDC	PAR
02	TCK	+12 VDC	23	AD27	AD26	44	C/BE1-	AD15
03	GND	TMS	24	AD25	GND	45	AD14	+3.3 VDC
04	TDO	TDI	25	+3.3 VDC	AD24	46	GND	AD13
05	+5 VDC	+5 VDC	26	C/BE3-	IDSEL	47	AD12	AD11
06	+5 VDC	INTA-	27	AD23	+3.3 VDC	48	AD10	GND
07	INTB-	INTC-	28	GND	AD22	49	GND	AD09
08	INTD-	+5 VDC	29	AD21	AD20	50	Key	Key
09	PRSNT1-	Reserved	30	AD19	GND	51	Key	Key
10	RSVD	+5 VDC	31	+3.3 VDC	AD18	52	AD08	C/BE0-
11	PRSNT2-	Reserved	32	AD17	AD16	53	AD07	+3.3 VDC
12	GND	GND	33	C/BE2-	+3.3 VDC	54	+3.3 VDC	AD06
13	GND	GND	34	GND	FRAME-	55	AD05	AD04
14	RSVD	+3.3 AUX	35	IRDY-	GND	56	AD03	GND
15	GND	RST-	36	+3.3 VDC	TRDY-	57	GND	AD02
16	CLK	+5 VDC	37	DEVSEL-	GND	58	AD01	AD00
17	GND	GNT-	38	GND	STOP-	59	+5 VDC	+5 VDC
18	REQ-	GND	39	LOCK-	+3.3 VDC	60	ACK64-	REQ64-
19	+5 VDC	PME-	40	PERR-	SDONE n	61	+5 VDC	+5 VDC
20	AD31	AD30	41	+3.3 VDC	SBO-	62	+5 VDC	+5 VDC
21	AD29	+3.3 VDC	42	SERR-	GND			

PCI Express Connectors

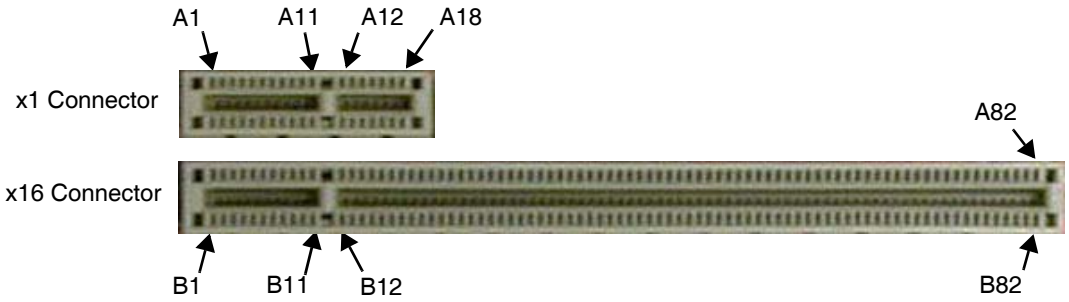


Figure 4-3. PCI Express Bus Connectors

Table 4-4.
PCI Express Bus Connector Pinout

Pin	B Signal	A Signal	Pin	B Signal	A Signal	Pin	B Signal	A Signal
01	+12 VDC	PRSNT1#	29	GND	PERp3	57	GND	PERn9
02	+12 VDC	+12 VDC	30	RSVD	PERn3	58	PETp10	GND
03	RSVD	+12 VDC	31	PRSNT2#	GND	59	PETn10	GND
04	GND	GND	32	GND	RSVD	60	GND	PERp10
05	SMCLK	+5 VDC	33	PETp4	RSVD	61	GND	PERn10
06	+5 VDC	JTAG2	34	PETn4	GND	62	PETp11	GND
07	GND	JTAG4	35	GND	PERp4	63	PETn11	GND
08	+3.3 VDC	JTAG5	36	GND	PERn4	64	GND	PERp11
09	JTAG1	+3.3 VDC	37	PETp5	GND	65	GND	PERn11
10	3.3 Vaux	+3.3 VDC	38	PETn5	GND	66	PETp12	GND
11	WAKE	PERST#	39	GND	PERp5	67	PETn12	GND
12	RSVD	GND	40	GND	PERn5	68	GND	PERp12
13	GND	REFCLK+	41	PETp6	GND	69	GND	PERn12
14	PETp0	REFCLK-	42	PETn6	GND	70	PETp13	GND
15	PETn0	GND	43	GND	PERp6	71	PETn13	GND
16	GND	PERp0	44	GND	PERn6	72	GND	PERp13
17	PRSNT2#	PERn0	45	PETp7	GND	73	GND	PERn13
18	GND	GND	46	PETn7	GND	74	PETp14	GND
19	PETp1	RSVD	47	GND	PERp7	75	PETn14	GND
20	PETn1	GND	48	PRSNT2#	PERn7	76	GND	PERp14
21	GND	PERp1	49	GND	GND	77	GND	PERn14
22	GND	PERn1	50	PETp8	RSVD	78	PETp15	GND
23	PETp2	GND	51	PETn8	GND	79	PETn15	GND
24	PETn2	GND	52	GND	PERp8	80	GND	PERp15
25	GND	PERp2	53	GND	PERn8	81	PRSNT2#	PERn15
26	GND	PERn2	54	PETp9	GND	82	RSVD	GND
27	PETp3	GND	55	PETn9	GND			
28	PETn3	GND	56	GND	PERp9			

4.3 System Resources

This section describes the availability and basic control of major subsystems, otherwise known as resource allocation or simply “system resources.” System resources are provided on a priority basis through hardware interrupts and DMA requests and grants.

4.3.1 Interrupts

The microprocessor uses two types of hardware interrupts; maskable and nonmaskable. A maskable interrupt can be enabled or disabled within the microprocessor by the use of the STI and CLI instructions. A nonmaskable interrupt cannot be masked off within the microprocessor, but may be inhibited by legacy hardware or software means external to the microprocessor.

The maskable interrupt is a hardware-generated signal used by peripheral functions within the system to get the attention of the microprocessor. Peripheral functions produce a unique INTA-H (PCI) or IRQ0-15 (ISA) signal that is routed to interrupt processing logic that asserts the interrupt (INTR-) input to the microprocessor. The microprocessor halts execution to determine the source of the interrupt and then services the peripheral as appropriate.

Most IRQs are routed through the I/O controller of the super I/O component, which provides the serializing function. A serialized interrupt stream is then routed to the ICH component.

Interrupts may be processed in one of two modes (selectable through the F10 Setup utility):

- 8259 mode
- APIC mode

These modes are described in the following subsections.

8259 Mode

The 8259 mode handles interrupts IRQ0-IRQ15 in the legacy (AT-system) method using 8259-equivalent logic. If more than one interrupt is pending, the highest priority (lowest number) is processed first.

APIC Mode

The Advanced Programmable Interrupt Controller (APIC) mode provides enhanced interrupt processing with the following advantages:

- Eliminates the processor's interrupt acknowledge cycle by using a separate (APIC) bus
- Programmable interrupt priority
- Additional interrupts (total of 24)

The APIC mode accommodates eight PCI interrupt signals (PIRQA-..PIRQH-) for use by PCI devices. The PCI interrupts are evenly distributed to minimize latency and wired as shown in Table 4-5.

Table 4-5.
PCI Interrupt Distribution

	System Interrupts							
System Board Connector	**PIRQ A**	**PIRQ B**	**PIRQ C**	**PIRQ D**	**PIRQ E**	**PIRQ F**	**PIRQ G**	**PIRQ H**
PCI slot 1 [1]					A	B	C	D
PCI slot 2 [1]					D	A	B	C
PCI slot 3 [2]					C	D	A	B

NOTES:

[1] SFF and CMT only
[2] CMT only

The PCI interrupts can be configured by PCI Configuration Registers 60h..63h to share the standard ISA interrupts (IRQn).

The APIC mode is supported by Windows NT, Windows 2000, and Windows XP, and Windows Vista operating systems. Systems running the Windows 95 or 98 operating system will need to run in 8259 mode.

4.3.2 Direct Memory Access

Direct Memory Access (DMA) is a method by which a device accesses system memory without involving the microprocessor. Although the DMA method has been traditionally used to transfer blocks of data to or from an ISA I/O device, PCI devices may also use DMA operation as well. The DMA method reduces the amount of CPU interactions with memory, freeing the CPU for other processing tasks. For detailed information regarding DMA operation, refer to the data manual for the Intel 82801 ICH9 I/O Controller Hub.

4.4 Real-Time Clock and Configuration Memory

The Real-time clock (RTC) and configuration memory (also referred to as "CMOS") functions are provided by the 82801 component and is MC146818-compatible. As shown in the following figure, the 82801 ICH9 component provides 256 bytes of battery-backed RAM divided into two 128-byte configuration memory areas. The RTC uses the first 14 bytes (00-0Dh) of the standard memory area. All locations of the standard memory area (00-7Fh) can be directly accessed using conventional OUT and IN assembly language instructions through I/O ports 70h/71h, although the suggested method is to use the INT15 AX=E823h BIOS call.

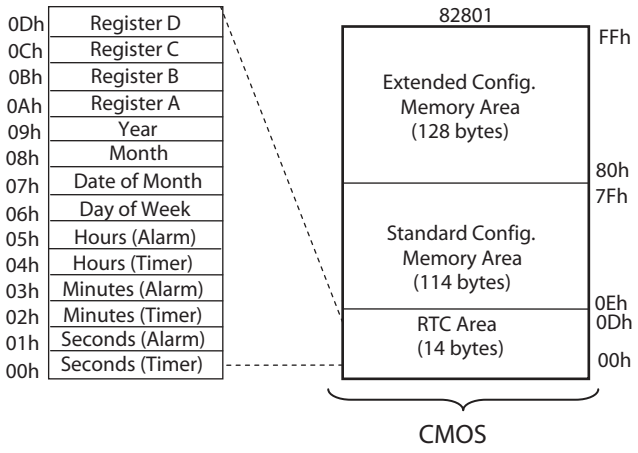


Figure 4 4. Configuration Memory Map

A lithium 3-VDC battery is used for maintaining the RTC and configuration memory while the system is powered down. During system operation a wire-Ored circuit allows the RTC and configuration memory to draw power from the power supply. The battery is located in a battery holder on the system board and has a life expectancy of three or more years. When the battery has expired it is replaced with a CR2032 or equivalent 3-VDC lithium battery.

4.4.1 Clearing CMOS

The contents of configuration memory (including the Power-On Password) can be cleared by the following procedure:

1. Turn off the unit.
2. Disconnect the AC power cord from the outlet and/or system unit.
3. Remove the chassis hood (cover) and insure that no LEDs on the system board are illuminated.
4. On the system board, press and hold the CMOS clear button (switch SW50, colored yellow) for at least 5 seconds.
5. Replace the chassis hood (cover).
6. Reconnect the AC power cord to the outlet and/or system unit.
7. Turn the unit on.

To clear only the Power-On Password refer to section 4.5.1.

4.4.2 Standard CMOS Locations

Table 4-6 describes standard configuration memory locations 0Ah-3Fh. These locations are accessible through using OUT/IN assembly language instructions using port 70/71h or BIOS function INT15, AX=E823h.

Table 4-6.
Configuration Memory (CMOS) Map

Location	Function	Location	Function
00-0Dh	Real-time clock	24h	System board ID
0Eh	Diagnostic status	25h	System architecture data
0Fh	System reset code	26h	Auxiliary peripheral configuration
10h	Diskette drive type	27h	Speed control external drive
11h	Reserved	28h	Expanded/base mem. size, IRQ12
12h	Hard drive type	29h	Miscellaneous configuration
13h	Security functions	2Ah	Hard drive timeout
14h	Equipment installed	2Bh	System inactivity timeout
15h	Base memory size, low byte/KB	2Ch	Monitor timeout, Num Lock Cntrl
16h	Base memory size, high byte/KB	2Dh	Additional flags
17h	Extended memory, low byte/KB	2Eh-2Fh	Checksum of locations 10h-2Dh
18h	Extended memory, high byte/KB	30h-31h	Total extended memory tested
19h	Hard drive 1, primary controller	32h	Century
1Ah	Hard drive 2, primary controller	33h	Miscellaneous flags set by BIOS
1Bh	Hard drive 1, secondary controller	34h	International language
1Ch	Hard drive 2, secondary controller	35h	APM status flags
1Dh	Enhanced hard drive support	36h	ECC POST test single bit
1Eh	Reserved	37h-3Fh	Power-on password
1Fh	Power management functions	40-FFh	Feature Control/Status

NOTES:

Assume unmarked gaps are reserved.

Higher locations (>3Fh) contain information that should be accessed using the INT15, AX=E845h BIOS function (refer to Chapter 8 for BIOS function descriptions).

4.5 System Management

This section describes functions having to do with security, power management, temperature, and overall status. These functions are handled by hardware and firmware (BIOS) and generally configured through the Setup utility.

4.5.1 Security Functions

These systems include various features that provide different levels of security. Note that this subsection describes only the hardware functionality (including that supported by Setup) and does not describe security features that may be provided by the operating system and application software.

Power-On / Setup Password

These systems include a power-on and setup passwords, which may be enabled or disabled (cleared) through a jumper on the system board. The jumper controls a GPIO input to the 82801 ICH9 that is checked during POST. The password is stored in configuration memory (CMOS) and if enabled and then forgotten by the user will require that either the password be cleared (preferable solution and described below) or the entire CMOS be cleared (refer to section 4.4.1).

To clear the password, use the following procedure:

1. Turn off the system and disconnect the AC power cord from the outlet and/or system unit.
2. Remove the cover (hood) as described in the appropriate User Guide or Maintainance And Service Reference Guide. Insure that all system board LEDs are off (not illuminated).
3. Locate the password clear jumper (header is colored green and labeled E49 on these systems) and move the jumper from pins 1 and 2 and place on (just) pin 2 (for safekeeping).
4. Replace the cover.
5. Re-connect the AC power cord to the AC outlet and/or system unit.
6. Turn on the system. The POST routine will clear and disable the password.
7. To re-enable the password feature, repeat steps 1-6, replacing the jumper on pins 1 and 2 of header E49.

Setup Password

The Setup utility may be configured to be always changeable or changeable only by entering a password. Refer to the previous procedure (Power On / Setup Password) for clearing the Setup password.

Cable Lock Provision

These systems include a chassis cutout (on the rear panel) for the attachment of a cable lock mechanism.

I/O Interface Security

The serial, parallel, USB, and diskette interfaces may be disabled individually through the Setup utility to guard against unauthorized access to a system. In addition, the ability to write to or boot from a removable media drive (such as the diskette drive) may be enabled through the Setup utility. The disabling of the serial, parallel, and diskette interfaces are a function of the SCH5317 I/O controller. The USB ports are controlled through the 82801.

Chassis Security

Some systems feature Smart Cover (hood) Sensor and Smart Cover (hood) Lock mechanisms to inhibit unauthorized tampering of the system unit.

Smart Cover Sensor

These systems include a plunger switch that, when the cover (hood) is removed, closes and grounds an input of the 82801 component. The battery-backed logic will record this “intrusion” event by setting a specific bit. This bit will remain set (even if the cover is replaced) until the system is powered up and the user completes the boot sequence successfully, at which time the bit will be cleared. Through Setup, the user can set this function to be used by Alert-On-LAN and or one of three levels of support for a “cover removed” condition:

Level 0—Cover removal indication is essentially disabled at this level. During POST, status bit is cleared and no other action is taken by BIOS.

Level 1—During POST the message "The computer's cover has been removed since the last system start up" is displayed and time stamp in CMOS is updated.

Level 2—During POST the "The computer's cover has been removed since the last system start up" message is displayed, time stamp in CMOS is updated, and the user is prompted for the administrator password. (A Setup password must be enabled in order to see this option).

Smart Cover Lock (Optional)

These systems support an optional solenoid-operated locking bar that, when activated, prevents the cover (hood) from being removed. The GPIO ports 44 and 45 of the SCH5317 I/O controller provide the lock and unlock signals to the solenoid. A locked hood may be bypassed by removing special screws that hold the locking mechanism in place. The special screws are removed with the Smart Cover Lock Failsafe Key.

4.5.2 Power Management

These systems provide baseline hardware support of ACPI- and APM-compliant firmware and software. Key power-consuming components (processor, chipset, I/O controller, and fan) can be placed into a reduced power mode either automatically or by user control. The system can then be brought back up ("wake-up") by events defined by the ACPI 2.0 specification. The ACPI wake-up events supported by this system are listed as follows:

Table 4-7.
ACPI Wake-Up Events

ACPI Wake-Up Event	System Wakes From
Power Button	Suspend or soft-off
RTC Alarm	Suspend or soft-off
Wake On LAN (w/NIC)	Suspend or soft-off
PME	Suspend or soft-off
Serial Port Ring	Suspend or soft-off
USB	Suspend only
Keyboard	Suspend only
Mouse	Suspend only

4.5.3 System Status

These systems provide a visual indication of system boot, ROM flash, and operational status through the power LED and internal speaker, as described in Table 4-8.

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Table 4-8.
System Operational Status LED Indications

System Status	PowerLED	Beeps [2]	Action Required
S0: System on (normal operation)	Steady green	None	None
S1: Suspend	Blinks green @ .5 Hz	None	None
S3: Suspend to RAM	Blinks green @ .5 Hz	None	None
S4: Suspend to disk	Off – clear	None	None
S5: Soft off	Off – clear	None	None
Processor thermal shutdown	Blinks red 2 times @ I Hz [1]	2	Check air flow, fans, heatsink
Processor not seated / installed	Blinks red 3 times @ I Hz [1]	3	Check processor presence/seating
Power supply overload failure	Blinks red 4 times @ I Hz [1]	4	Check system board problem [3],
Memory error (pre-video)	Blinks red 5 times @ I Hz [1]	5	Check DIMMs, system board
Video error	Blinks red 6 times @ I Hz [1]	6	Check graphics card or system board
PCA failure detected by BIOS (pre-video)	Blinks red 7 times @ I Hz [1]	7	Replace system board
Invalid ROM checksum error	Blinks red 8 times @ I Hz [1]	8	Reflash BIOS ROM
Boot failure (after power on)	Blinks red 9 times @ I Hz [1]	9	Check power supply, processor, sys. bd
Bad option card	Blinks red 10 times @ I Hz [1]	None	Replace option card

NOTES:

Beeps are repeated for 5 cycles, after which only blinking LED indication continues.

[1] Repeated after 2 second pause.

[2] Beeps are produced by the internal chassis speaker.

[3] Check that CPU power connector P3 is plugged in.

4.5.4 Thermal Sensing and Cooling

All systems feature a variable-speed fan mounted as part of the processor heatsink assembly. All systems also provide or support an auxiliary chassis fan. All fans are controlled through temperature sensing logic on the system board and/or in the power supply. There are some electrical differences between form factors and between some models, although the overall functionally is the same. Typical cooling conditions include the following:

1. Normal—Low fan speed.
2. Hot processor—ASIC directs Speed Control logic to increase speed of fan(s).
3. Hot power supply—Power supply increases speed of fan(s).
4. Sleep state—Fan(s) turned off. Hot processor or power supply will result in starting fan(s).

The RPM (speed) of all fans is the result of the temperature of the CPU as sensed by speed control circuitry. The fans are controlled to run at the slowest (quietest) speed that will maintain proper cooling.

Units using chassis and CPU fans must have both fans connected to their corresponding headers to ensure proper cooling of the system.

4.6 Register Map and Miscellaneous Functions

This section contains the system I/O map and information on general-purpose functions of the ICH9 and I/O controller.

4.6.1 System I/O Map

Table 4-9 lists the fixed addresses of the input/output (I/O) ports.

Table 4-9
System I/O Map

I/O Port	Function
0000..001Fh	DMA Controller 1
0020..002Dh	Interrupt Controller 1
002E, 002Fh	Index, Data Ports to SCH5317 I/O Controller (primary)
0030..003Dh	Interrupt Controller
0040..0042h	Timer 1
004E, 004Fh	Index, Data Ports to SCH5317 I/O Controller (secondary)
0050..0052h	Timer / Counter
0060..0067h	Microcontroller, NMI Controller (alternating addresses)
0070..0077h	RTC Controller
0080..0091h	DMA Controller
0092h	Port A, Fast A20/Reset Generator
0093..009Fh	DMA Controller
00A0..00B1h	Interrupt Controller 2
00B2h, 00B3h	APM Control/Status Ports
00B4..00BDh	Interrupt Controller
00C0..00DFh	DMA Controller 2
00F0h	Coprocessor error register
0170..0177h	IDE Controller 2 (active only if standard I/O space is enabled for secondary controller)
01F0..01F7h	IDE Controller 1 (active only if standard I/O space is enabled for primary controller)
0278..027Fh	Parallel Port (LPT2)
02E8..02EFh	Serial Port (COM4)
02F8..02FFh	Serial Port (COM2)
0370..0377h	Diskette Drive Controller Secondary Address
0376h	IDE Controller 2 (active only if standard I/O space is enabled for primary drive)
0378..037Fh	Parallel Port (LPT1)
03B0..03DFh	Graphics Controller
03BC..03BEh	Parallel Port (LPT3)
03E8..03EFh	Serial Port (COM3)
03F0..03F5h	Diskette Drive Controller Primary Addresses
03F6h	IDE Controller 1 (active only if standard I/O space is enabled for sec. drive)
03F8..03FFh	Serial Port (COM1)
04D0, 04D1h	Interrupt Controller
0678..067Fh	Parallel Port (LPT2)
0778..077Fh	Parallel Port (LPT1)
07BC..07BEh	Parallel Port (LPT3)
0CF8h	PCI Configuration Address (dword access only)
0CF9h	Reset Control Register
0CFCh	PCI Configuration Data (byte, word, or dword access)

NOTE:

Assume unmarked gaps are unused, reserved, or used by functions that employ variable I/O address mapping. Some ranges may include reserved addresses.

4.6.2 GPIO Functions

ICH9 Functions

The ICH9 provides various functions through the use of programmable general purpose input/output (GPIO) ports. These systems use GPIO ports and associate registers of the ICH9 for the following functions:

- PCI interupt request control

- Chassis and board ID
- Hood (cover) sensor and lock detect
- Media card reader detect
- S4 state indicator
- USB port over-current detect
- Flash security override
- Serial port detect
- REQn#/GNTn# sigal control
- Password enable
- Boot block enable

I/O Controller Functions

In addition to the serial and parallel port functions, the SCH5327 I/O controller provides the following specialized functions through GPIO ports:

- Power/Hard drive LED control for indicating system events (refer to Table 4-8)
- Hood lock/unlock controls the lock bar mechanism
- Thermal shutdown control turns off the CPU when temperature reaches certain level
- Processor present/speed detection detects if the processor has been removed. The occurrence of this event will, during the next boot sequence, initiate the speed selection routine for the processor.
- Legacy/ACPI power button mode control uses the pulse signal from the system's power button and produces the PS On signal according to the mode (legacy or ACPI) selected. Refer to chapter 7 for more information regarding power management.

5

Input/Output Interfaces

5.1 Introduction

This chapter describes the standard interfaces that provide input and output (I/O) porting of data and that are controlled through I/O-mapped registers. The following I/O interfaces are covered in this chapter:

- SATA interface (5.2)
- PATA interface (5.3)
- Diskette drive interface (5.4)
- Serial interfaces (5.5)
- Parallel interface (5.6)
- Keyboard/pointing device interface (5.7)
- Universal serial bus interface (5.8)
- Audio subsystem (5.9)
- Network interface controller (5.10)

5.2 SATA Interface

These systems provide one, three, or four serial ATA (SATA) interfaces that support tranfer rates up to 3.0 Gb/s and RAID data protection functionality. The SATA interface duplicates most of the functionality of the EIDE interface through a register interface that is equivalent to that of the legacy IDE host adapter.

The ICH9 DO component includes Intel RAID migration technology that simplifies the migration from a single hard to a RAID0 or RAID1 dual hard drive array without requiring OS reinstallation. Intel Matrix RAID provides exceptional storage performance with increased data protection for configurations using dual drive arrays. A software solution is included that provides full management and status reporting of the RAID array, and the BIOS ROM also supports RAID creation, naming, and deletion of RAID arrays.

The standard 7-pin SATA connector is shown in the figure below.

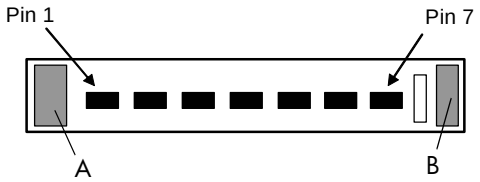


Figure 5-1. 7-Pin SATA Connector (P60-P63 on system board).

Table 5-1.
7-Pin SATA Connector Pinout

Pin	Description	Pin	Description
1	Ground	6	RX positive
2	TX positive	7	Ground
3	TX negative	A	Holding clip
4	Ground	B	Holding clip
5	RX negative	--	--

The USDT system includes a notebook-type SATA connector (J102) that mates directly (i.e., without a cable) to a 2.5-inch mass storage device.

5.3 PATA Interface

The USDT system board includes a SATA-to-PATA bridge and slim IDE connector that supports an IDE-type optical disk drive. The pinout for this connector is listed in Table 5-2

The 44-pin slim IDE connector is shown in the figure below.

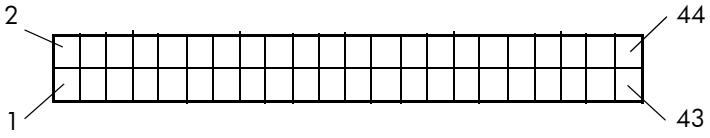


Figure 5-2. 44-pin Slim IDE Connector (P21on system board).

Table 5-2.
44-Pin Slim IDE Connector Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	RESET#	2	GND	23	DIOW#	24	GND
3	DD7	4	DD8	25	DIOR#	26	GND
5	DD6	6	DD9	27	IORDY	28	CSEL
7	DD5	8	DD10	29	DMACK#	30	GND
9	DD4	10	DD11	31	INTRQ	32	NC
11	DD3	12	DD12	33	DA1	34	PDIAG#
13	DD2	14	DD13	35	DA0	36	DA2
15	DD1	16	DD14	37	CS0#	38	CS1#
17	DD0	18	DD15	39	IDEACT#	40	GND
19	GND	20	Key (no pin)	41	5V	42	5V
21	DMARQ	22	GND	43	GND	44	Reserved

5.4 Diskette Drive Interface

The SFF and CMT form factors support a diskette drive through a standard 34-pin diskette drive connector. Selected models come standard with a 3.5-inch 1.44-MB diskette drive installed as drive A.

The diskette drive interface function is integrated into the SCH5317 super I/O component. The internal logic of the I/O controller is software-compatible with standard 82077-type logic. The diskette drive controller has three operational phases in the following order:

- Command phase—The controller receives the command from the system.
- Execution phase—The controller carries out the command.
- Results phase—Status and results data is read back from the controller to the system.

The Command phase consists of several bytes written in series from the CPU to the data register (3F5h/375h). The first byte identifies the command and the remaining bytes define the parameters of the command. The Main Status register (3F4h/374h) provides data flow control for the diskette drive controller and must be polled between each byte transfer during the Command phase.

The Execution phase starts as soon as the last byte of the Command phase is received. An Execution phase may involve the transfer of data to and from the diskette drive, a mechnical control function of the drive, or an operation that remains internal to the diskette drive controller.

Data transfers (writes or reads) with the diskette drive controller are by DMA, using the DRQ2 and DACK2- signals for control.

The Results phase consists of the CPU reading a series of status bytes (from the data register (3F5h/375h)) that indicate the results of the command. Note that some commands do not have a Result phase, in which case the Execution phase can be followed by a Command phase.

During periods of inactivity, the diskette drive controller is in a non-operation mode known as the Idle phase.

The SFF and CMT form factors use a standard 34-pin connector for diskette drives (refer to Figure 5-3 and Table 5-3 for the pinout). Drive power is supplied through a separate connector.

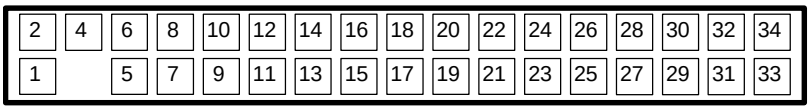


Figure 5-3. 34-Pin Diskette Drive Connector (P10 on system board).

Table 5-3.
34-Pin Diskette Drive Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	18	DIR-	Drive head direction control
2	LOW DEN-	Low density select	19	GND	Ground
3	---	(KEY)	20	STEP-	Drive head track step cntrl.
4	MEDIA ID-	Media identification	21	GND	Ground
5	GND	Ground	22	WR DATA-	Write data
6	DRV 4 SEL-	Drive 4 select	23	GND	Ground
7	GND	Ground	24	WR ENABLE-	Enable for WR DATA-
8	INDEX-	Media index is detected	25	GND	Ground
9	GND	Ground	26	TRK 00-	Heads at track 00 indicator
10	MTR 1 ON-	Activates drive motor	27	GND	Ground
11	GND	Ground	28	WR PRTK-	Media write protect status
12	DRV 2 SEL-	Drive 2 select	29	GND	Ground
13	GND	Ground	30	RD DATA-	Data and clock read off disk
14	DRV 1 SEL-	Drive 1 select	31	GND	Ground
15	GND	Ground	32	SIDE SEL-	Head select (side 0 or 1)
16	MTR 2 ON-	Activates drive motor	33	GND	Ground
17	GND	Ground	34	DSK CHG-	Drive door opened indicator

5.5 Serial Interface

Systems covered in this guide may include one RS-232-C type serial interface to transmit and receive asynchronous serial data with external devices. Some systems may allow the installation of a second serial interface through an adapter that consists of a PCI bracket and a cable that attaches to header P52 on the system board. The serial interface function is provided by the SCH5317 I/O controller component that includes two NS16C550-compatible UARTs.

The UART supports the standard baud rates up through 115200, and also special high speed rates of 239400 and 460800 baud. The baud rate of the UART is typically set to match the capability of the connected device. While most baud rates may be set at runtime, baud rates 230400 and 460800 must be set during the configuration phase.

The serial interface uses a DB-9 connector as shown in the following figure with the pinout listed in Table 5-4.

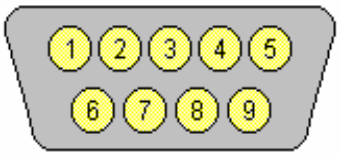


Figure 5-4. DB-9 Serial Interface Connector (as viewed from rear of chassis)

Table 5-4.
DB-9 Serial Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	CD	Carrier Detect	6	DSR	Data Set Ready
2	RX Data	Receive Data	7	RTS	Request To Send
3	TX Data	Transmit Data	8	CTS	Clear To Send
4	DTR	Data Terminal Ready	9	RI	Ring Indicator
5	GND	Ground	-	-	-

The standard RS-232-C limitation of 50 feet (or less) of cable between the DTE (computer) and DCE (modem) should be followed to minimize transmission errors. Higher baud rates may require shorter cables.

5.6 Parallel Interface

Systems covered in this guide may include a parallel interface for connection to a peripheral device with a compatible interface, the most common being a printer. The parallel interface function is integrated into the SCH5317 I/O controller component and provides bi-directional 8-bit parallel data transfers with a peripheral device. The parallel interface supports three main modes of operation:

- Standard Parallel Port (SPP) mode
- Enhanced Parallel Port (EPP) mode
- Extended Capabilities Port (ECP) mode

These three modes (and their submodes) provide complete support as specified for an IEEE 1284 parallel port.

5.6.1 Standard Parallel Port Mode

The Standard Parallel Port (SPP) mode uses software-based protocol and includes two sub-modes of operation, compatible and extended, both of which can provide data transfers up to 150 KB/s. In the compatible mode, CPU write data is simply presented on the eight data lines. A CPU read of the parallel port yields the last data byte that was written.

5.6.2 Enhanced Parallel Port Mode

In Enhanced Parallel Port (EPP) mode, increased data transfers are possible (up to 2 MB/s) due to a hardware protocol that provides automatic address and strobe generation. EPP revisions 1.7 and 1.9 are both supported. For the parallel interface to be initialized for EPP mode, a negotiation phase is entered to detect whether or not the connected peripheral is compatible with EPP mode. If compatible, then EPP mode can be used. In EPP mode, system timing is closely coupled to EPP timing. A watchdog timer is used to prevent system lockup.

5.6.3 Extended Capabilities Port Mode

The Extended Capabilities Port (ECP) mode, like EPP, also uses a hardware protocol-based design that supports transfers up to 2 MB/s. Automatic generation of addresses and strobes as well as Run Length Encoding (RLE) decompression is supported by ECP mode. The ECP mode includes a bi-directional FIFO buffer that can be accessed by the CPU using DMA or programmed I/O. For the parallel interface to be initialized for ECP mode, a negotiation phase is entered to detect whether or not the connected peripheral is compatible with ECP mode. If compatible, then ECP mode can be used.

The ECP mode includes several sub-modes as determined by the Extended Control register. Two submodes of ECP allow the parallel port to be controlled by software. In these modes, the FIFO is cleared and not used, and DMA and RLE are inhibited.

5.6.4 Parallel Interface Connector

Figure 5-5 and Table 5-5 show the connector and pinout of the parallel interface connector. Note that some signals are redefined depending on the port's operational mode.

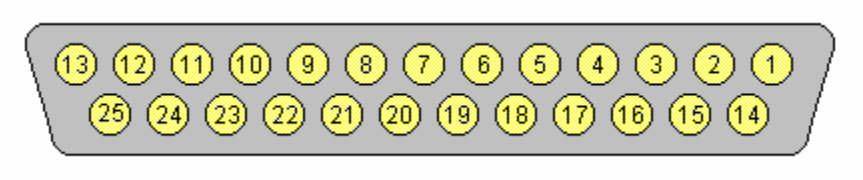


Figure 5-5. DB-25 Parallel Interface Connector (as viewed from rear of chassis)

Table 5-5.
DB-25 Parallel Connector Pinout

Pin	Signal	Function	Pin	Signal	Function
1	STB-	Strobe / Write [1]	14	LF-	Line Feed [2]
2	D0	Data 0	15	ERR-	Error [3]
3	D1	Data 1	16	INIT-	Initialize Paper [4]
4	D2	Data 2	17	SLCTIN-	Select In / Address. Strobe [1]
5	D3	Data 3	18	GND	Ground
6	D4	Data 4	19	GND	Ground
7	D5	Data 5	20	GND	Ground
8	D6	Data 6	21	GND	Ground
9	D7	Data 7	22	GND	Ground
10	ACK-	Acknowledge / Interrupt [1]	23	GND	Ground
11	BSY	Busy / Wait [1]	24	GND	Ground
12	PE	Paper End / User defined [1]	25	GND	Ground
13	SLCT	Select / User defined [1]	--	--	--

NOTES:

[1] Standard and ECP mode function / EPP mode function

[2] EPP mode function: Data Strobe
ECP modes: Auto Feed or Host Acknowledge

[3] EPP mode: user defined
ECP modes:Fault or Peripheral Req.

[4] EPP mode: Reset
ECP modes: Initialize or Reverse Req.

5.7 Keyboard/Pointing Device Interface

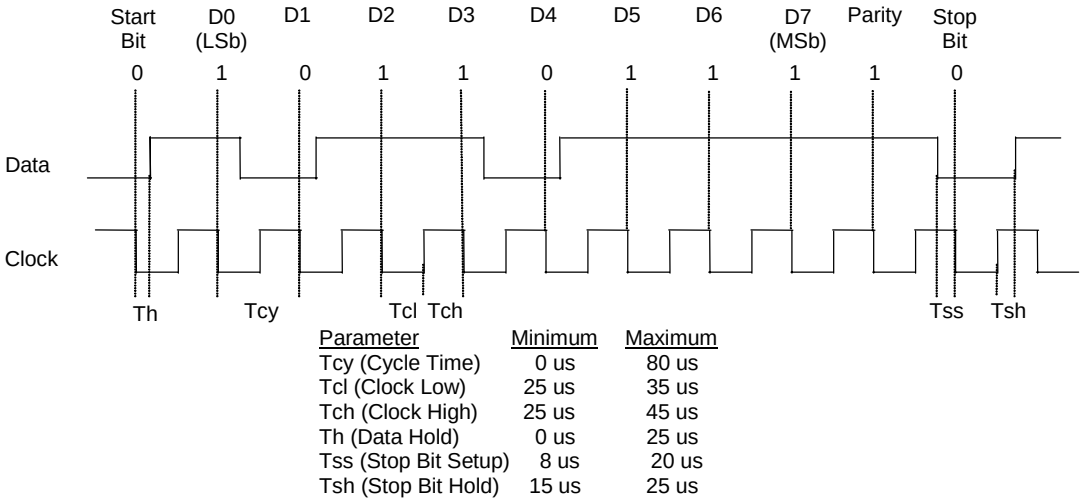
The keyboard/pointing device interface function is provided by the SCH5317 I/O controller component, which integrates 8042-compatible keyboard controller logic (hereafter referred to as simply the "8042") to communicate with the keyboard and pointing device using bi-directional serial data transfers. The 8042 handles scan code translation and password lock protection for the keyboard as well as communications with the pointing device.

5.7.1 Keyboard Interface Operation

The data/clock link between the 8042 and the keyboard is uni-directional for Keyboard Mode 1 and bi-directional for Keyboard Modes 2 and 3. (These modes are discussed in detail in Appendix C). This section describes Mode 2 (the default) mode of operation.

Communication between the keyboard and the 8042 consists of commands (originated by either the keyboard or the 8042) and scan codes from the keyboard. A command can request an action or indicate status. The keyboard interface uses IRQ1 to get the attention of the CPU.

The 8042 can send a command to the keyboard at any time. When the 8042 wants to send a command, the 8042 clamps the clock signal from the keyboard for a minimum of 60 us. If the keyboard is transmitting data at that time, the transmission is allowed to finish. When the 8042 is ready to transmit to the keyboard, the 8042 pulls the data line low, causing the keyboard to respond by pulling the clock line low as well, allowing the start bit to be clocked out of the 8042. The data is then transferred serially, LSb first, to the keyboard (Figure 5-6). An odd parity bit is sent following the eighth data bit. After the parity bit is received, the keyboard pulls the data line low and clocks this condition to the 8042. When the keyboard receives the stop bit, the clock line is pulled low to inhibit the keyboard and allow it to process the data.



Parameter	Minimum	Maximum
Tcy (Cycle Time)	0 us	80 us
Tcl (Clock Low)	25 us	35 us
Tch (Clock High)	25 us	45 us
Th (Data Hold)	0 us	25 us
Tss (Stop Bit Setup)	8 us	20 us
Tsh (Stop Bit Hold)	15 us	25 us

Figure 5-6. 8042-To-Keyboard Transmission of Code EDh, Timing Diagram

Control of the data and clock signals is shared by the 8042 and the keyboard depending on the originator of the transferred data. Note that the clock signal is always generated by the keyboard.

After the keyboard receives a command from the 8042, the keyboard returns an ACK code. If a parity error or timeout occurs, a Resend command is sent to the 8042.

5.7.2 Pointing Device Interface Operation

The pointing device (typically a mouse) connects to a 6-pin DIN-type connector that is identical to the keyboard connector both physically and electrically. The operation of the interface (clock and data signal control) is the same as for the keyboard. The pointing device interface uses the IRQ12 interrupt.

5.7.3 Keyboard/Pointing Device Interface Connector

The legacy-light model provides separate PS/2 connectors for the keyboard and pointing device. Both connectors are identical both physically and electrically. Figure 5-7 and Table 5-6 show the connector and pinout of the keyboard/pointing device interface connectors.

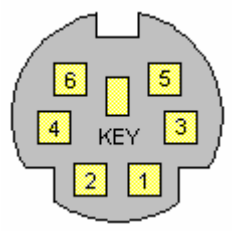


Figure 5-7. PS/2 Keyboard or Pointing Device Interface Connector (as viewed from rear of chassis)

Table 5-6.
Keyboard/Pointing Device Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	DATA	Data	4	+ 5 VDC	Power
2	NC	Not Connected	5	CLK	Clock
3	GND	Ground	6	NC	Not Connected

5.8 Universal Serial Bus Interface

The Universal Serial Bus (USB) interface provides asynchronous/isochronous data transfers with compatible peripherals such as keyboards, printers, or modems. This high-speed interface supports hot-plugging of compatible devices, making possible system configuration changes without powering down or even rebooting systems.

These systems provide eight externally-accessible USB ports, two front panel USB ports (which may be disabled) and six USB ports on the rear panel. In addition, the SFF and CMT form factors support a media reader accessory that uses two USB ports through a system board connection. The USB ports are dynamically configured to either a USB 1.1 controller or the USB 2.0 controller depending on the capability of the peripheral device. The 1.1 controllers provide a maximum transfer rate of 12 Mb/s while the 2.0 controller provides a maximum transfer rate of 480 Mb/s. Table 5-7 shows the mapping of the USB ports.

Table 5-7.
ICH9 USB Port Mapping

ICH9 Controller	Signals	USB Connector Location	
		USDT, SFF Form Factors	CMT Form Factor
USB 1.1 #1, USB 2.0 #1	Data 0P, 0N	System board header P150	Rear panel dual USB stack w/RJ-45
	Data 1P, 1N	System board header P150	Rear panel dual USB stack w/RJ-45
USB 1.1 #2 USB 2.0 #1	Data 2P, 2N	Front panel USB	Rear panel quad USB stack
	Data 3P, 3N	Front panel USB	Rear panel quad USB stack
USB 1.1 #3 USB 2.0 #1	Data 4P, 4N	Not used	Rear panel quad USB stack
	Data 5P, 5N	Not used	Rear panel quad USB stack
USB 1.1 #4 USB 2.0 #2	Data 6P, 6N	Rear panel quad USB stack	system board header P150
	Data 7P, 7N	Rear panel quad USB stack	system board header P150
USB 1.1 #5 USB 2.0 #2	Data 8P, 8N	Rear panel quad USB stack	Front panel USB
	Data 9P, 9N	Rear panel quad USB stack	Front panel USB
USB 1.1 #6 USB 2.0 #2	Data 10P, 10N	Rear panel dual USB stack w/RJ-45	Not used
	Data 11P, 11N	Rear panel dual USB stack w/RJ-45	Not used

5.8.1 USB Connector

These systems provide type-A USB ports as shown in Figure 5-7.

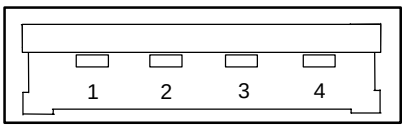


Figure 5-8. Universal Serial Bus Connector (as viewed from rear of chassis)

Table 5-8.
USB Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	Vcc	+5 VDC	3	USB+	Data (plus)
2	USB-	Data (minus)	4	GND	Ground

5.8.2 USB Cable Data

The recommended cable length between the host and the USB device should be no longer than sixteen feet for full-channel (12 MB/s) operation, depending on cable specification (see following table).

Table 5-9.
USB Cable Length Data

Conductor Size	Resistance	Maximum Length
20 AWG	0.036 Ω	16.4 ft (5.00 m)
22 AWG	0.057 Ω	9.94 ft (3.03 m)
24 AWG	0.091 Ω	6.82 ft (2.08 m)
26 AWG	0.145 Ω	4.30 ft (1.31 m)
28 AWG	0.232 Ω	2.66 ft (0.81 m)

NOTE:

For sub-channel (1.5 MB/s) operation and/or when using sub-standard cable shorter lengths may be allowable and/or necessary.

The shield, chassis ground, and power ground should be tied together at the host end but left unconnected at the device end to avoid ground loops.

Table 5-10.
USB Color Code

Signal	Insulation color
Data +	Green
Data -	White
Vcc	Red
Ground	Black

5.9 Audio Subsystem

These systems use the HD audio controller of the 82801 component to access and control an Analog Devices AD1884 HD Audio Codec, which provides 2-channel high definition analog-to-digital (ADC) and digital-to-analog (DAC) conversions. A block diagram of the audio subsystem is shown in Figure 5-9. All control functions such as volume, audio source selection, and sampling rate are controlled through software through the HD Audio Interface of the 82801 ICH component. Control data and digital audio streams (record and playback) are transferred between the ICH and the Audio Codec over the HD Audio Interface. The codec's speaker output is applied to a 1.5-watt amplifier that drives the internal speaker. A device plugged into the Headphone jack or the line input jack is sensed by the system, which will inhibit the Speaker Audio signal.

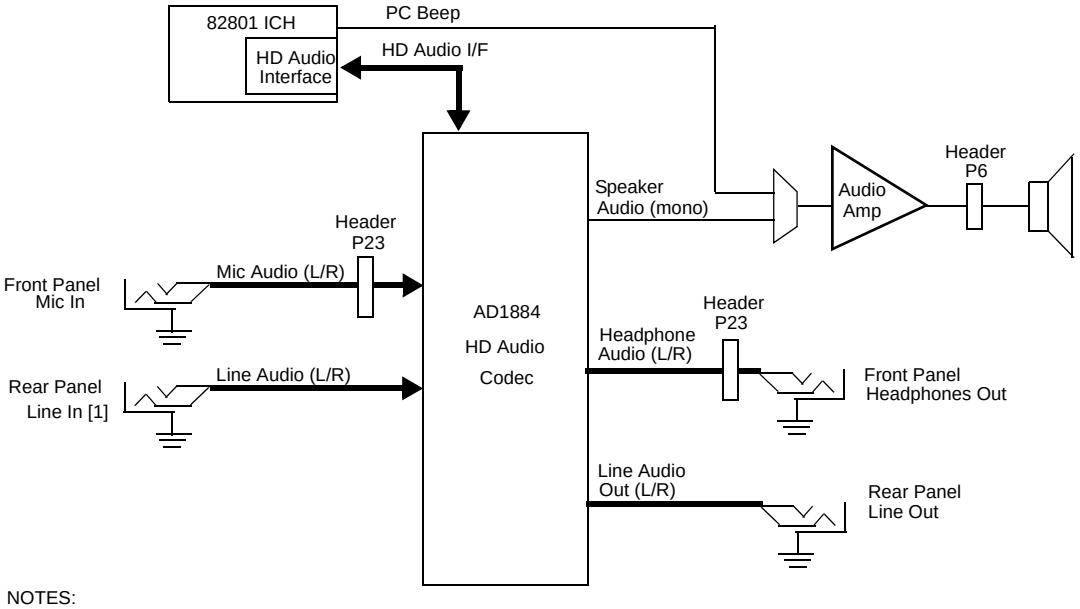
These systems provide the following analog interfaces for external audio devices:

Microphone In—This input uses a three-conductor 1/8-inch mini-jack that accepts a stereo microphone.

Line In—This input uses a three-conductor (stereo) 1/8-inch mini-jack designed for connection of a high-impedance audio source such as a tape deck. This jack can be re-tasked to a Microphone In function.

Headphones Out—This input uses a three-conductor (stereo) 1/8-inch mini-jack that is designed for connecting a set of 32-ohm (nom.) stereo headphones. Plugging into the Headphones jack mutes the signal to the internal speaker and the Line Out jack as well.

Line Out—This output uses a three-conductor (stereo) 1/8-inch mini-jack for connecting left and right channel line-level signals. Typical connections include a tape recorder's Line In (Record In) jacks, an amplifier's Line In jacks, or to powered speakers that contain amplifiers.



NOTES:

L/R = Separate left and right channels (stereo). L+R = Combined left and right channels (mono).

[1] Can be re-configured as Microphone In

Figure 5-9. Audio Subsystem Functional Block Diagram

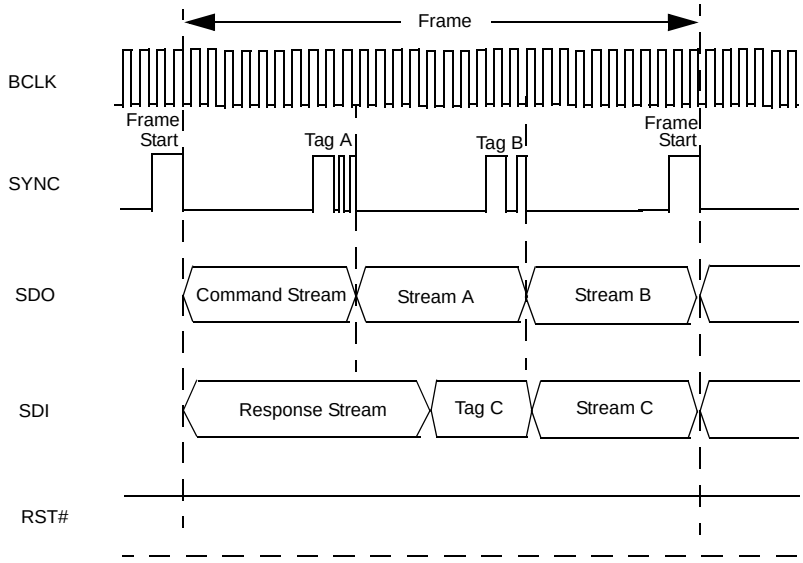
5.9.1 HD Audio Controller

The HD Audio Controller is a PCI Express device that is integrated into the 82801 ICH component and supports the following functions:

- Read/write access to audio codec registers
- Support for greater than 48-KHz sampling
- HD audio interface

5.9.2 HD Audio Link Bus

The HD audio controller and the HD audio codec communicate over a five-signal HD Audio Link Bus (Figure 5-10). The HD Audio Interface includes two serial data lines; serial data out (SDO, from the controller) and serial data in (SDI, from the audio codec) that transfer control and PCM audio data serially to and from the audio codec using a time-division multiplexed (TDM) protocol. The data lines are qualified by the 24-MHz BCLK signal driven by the audio controller. Data is transferred in frames synchronized by the 48-KHz SYNC signal, which is derived from the clock signal and driven by the audio controller. When asserted (typically during a power cycle), the RESET- signal (not shown) will reset all audio registers to their default values.



NOTE: Clock not drawn to scale.

Figure 5-10. HD Audio Link Bus Protocol

5.9.3 Audio Multistreaming

The audio subsystem can be configured (through the ADI control panel) for processing audio for multiple applications. The Headphone Out jack can provide audio for one application while the Line Out jack can provide external speaker audio from another application.

5.9.4 Audio Specifications

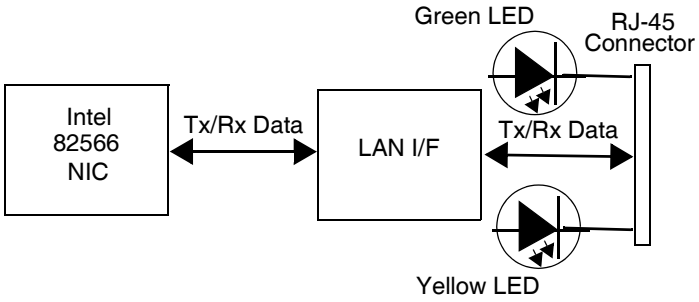
The specifications for the HD Audio subsystem are listed in Table 5-11.

Table 5-11.
HD Audio Subsystem Specifications

Parameter	Measurement
Sampling Rates:	
DAC	44.1-, 48-, 96-, & 192-KHz
ADC	44.1-, 48-, 96-, & 192KHz
Resolution:	
DAC	24-bit
ADC	24-bit
Nominal Input Voltage:	
Mic In (w/+20 db gain)	.283 Vp-p
Line In	2.83 Vp-p
Subsystem Impedance:	
Mic In	20K ohms
Line In	20K ohms
Line Out (minimum expected load)	10K ohms
Headphones Out (minimum expected load)	32 ohms
Signal-to-Noise Ratio	
Line out	90 db (nom)
Headphone out	90 db (nom)
Microphone / line in	85 db (nom)
Total Harmonic Distortion (THD)	
Line out	-84 db
Headphone out	-80 db
Microphone / line in	-78 db
Max. Subsystem Power Output to 4-ohm Internal Speaker (with 10% THD):	1.5 watts
Gain Step	1.5 db
Master Volume Range	-58.5 db
Frequency Response:	
ADC/DAC	20– 20000 Hz
Internal Speaker	450–20000 Hz

5.10 Network Interface Controller

These systems provide 10/100/1000 Mbps network support through an Intel 82566 network interface controller (NIC), a PHY component, and a RJ-45 jack with integral status LEDs. The 82562-equivalent controller integrated into the 82801 ICH component is not used (disabled) in these systems. (Figure 5-11). The support firmware for the BCM5752 component is contained in the system (BIOS) ROM. The NIC can operate in half- or full-duplex modes, and provides auto-negotiation of both mode and speed. Half-duplex operation features an Intel-proprietary collision reduction mechanism while full-duplex operation follows the IEEE 802.3x flow control specification.



LED	Function
Green	Activity/Link. Indicates network activity and link pulse reception.
Yellow	Speed: Off = 10 Mb/s, yellow = 100Mb/s, green = 1 Gb/s.

Figure 5-11. Network Interface Controller Block Diagram

The Network Interface Controller includes the following features:

- VLAN tagging with Windows XP and Linux
- Multiple VLAN support with Windows XP
- Power management support for ACPI 1.1, PXE 2.0, WOL, ASF 1.0, IPMI, AMT 3.0
- Cisco Etherchannel support
- Link and Activity LED indicator drivers

The controller features high and low priority queues and provides priority-packet processing for networks that can support that feature. The controller's micro-machine processes transmit and receive frames independently and concurrently. Receive runt (under-sized) frames are not passed on as faulty data but discarded by the controller, which also directly handles such errors as collision detection or data under-run.

The NIC uses 3.3 VDC auxiliary power, which allows the controller to support Wake-On-LAN (WOL) and Alert-On-LAN (AOL) functions while the main system is powered down.

For the features in the following paragraphs to function as described, the system unit must be plugged into a live AC outlet. Controlling unit power through a switchable power strip will, with the strip turned off, disable any wake, alert, or power mangement functionality.

5.10.1 Wake-On-LAN Support

The NIC supports the Wired-for-Management (WfM) standard of Wake-On-LAN (WOL) that allows the system to be booted up from a powered-down or low-power condition upon the detection of special packets received over a network. The NIC receives 3.3 VDC auxiliary power while the system unit is powered down in order to process special packets. The detection of a Magic Packet by the NIC results in the PME- signal on the PCI bus to be asserted, initiating system wake-up from an ACPI S1 or S3 state.

5.10.2 Alert Standard Format Support

Alert Standard Format (ASF) support allows the NIC to communicate the occurrence of certain events over a network to an ASF 1.0-compliant management console and, if necessary, take action that may be required. The ASF communications can involve the following:

- Alert messages sent by the client to the management console.
- Maintenance requests sent by the management console to the client.
- Description of client's ASF capabilities and characteristics.

The activation of ASF functionality requires minimal intervention of the user, typically requiring only booting a client system that is connected to a network with an ASF-compliant management console.

5.10.3 Power Management Support

The NIC features Wired-for-Management (WfM) support providing system wake up from network events (WOL) as well as generating system status messages (AOL) and supports ACPI power management environments. The controller receives 3.3 VDC (auxiliary) power as long as the system is plugged into a live AC receptacle, allowing support of wake-up events occurring over a network while the system is powered down or in a low-power state.

The Advanced Configuration and Power Interface (ACPI) functionality of system wake up is implemented through an ACPI-compliant OS and is the default power management mode. The following wakeup events may be individually enabled/disabled through the supplied software driver:

- Magic Packet—Packet with node address repeated 16 times in data portion

The following functions are supported in NDIS5 drivers but implemented through remote management software applications (such as LanDesk).

- Individual address match—Packet with matching user-defined byte mask
- Multicast address match—Packet with matching user-defined sample frame
- ARP (address resolution protocol) packet
- Flexible packet filtering—Packets that match defined CRC signature

The PROSet Application software (pre-installed and accessed through the System Tray or Windows Control Panel) allows configuration of operational parameters such as WOL and duplex mode.

5.10.4 NIC Connector

Figure 5-12 shows the RJ-45 connector used for the NIC interface. This connector includes the two status LEDs as part of the connector assembly.

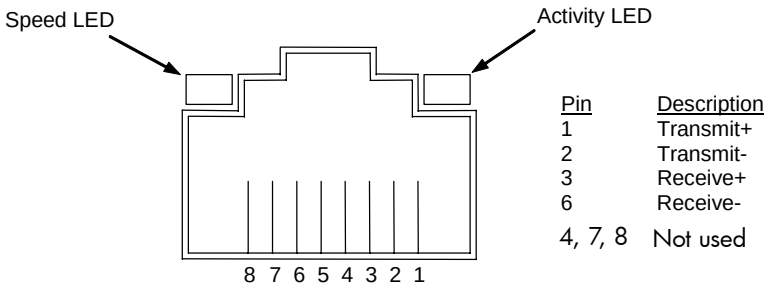


Figure 5-12. RJ-45 Ethernet TPE Connector (as viewed from rear of chassis)

5.10.5 NIC Specifications

Table 5-12.
NIC Specifications

Parameter	Compatibility standard orprotocol
Modes Supported	10BASE-T half duplex @ 10 Mb/s 10Base-T full duplex @ 20 Mb/s 100BASE-TX half duplex @ 100 Mb/s 100Base-TX full duplex @ 200 Mb/s 1000BASE-T half duplex @ 1 Gb/s 1000BASE-TX full duplex @ 2 Gb/s
Standards Compliance	IEEE 802.1P, 802.1Q IEEE 802.2 IEEE 802.3, 802.3ab, 802.3ad, 802.3u, 802.3x, 802.3z
OS Driver Support	MS-DOS MS Windows 3.1 MS Windows 95 (pre-OSR2), 98, and 2000 Professional, XP Home, XP Pro, Vista Home, Vista Pro MS Windows NT 3.51 & 4.0 Novell Netware 3.x, 4.x, 5x Novell Netware/IntraNetWare SCO UnixWare 7 Linux 2.2, 2.4 PXE 2.0
Boot ROM Support	Intel PRO/100 Boot Agent (PXE 3.0, RPL)
F12 BIOS Support	Yes
Bus Inteface	PCI Express x1
Power Management Support	ACPI, PCI Power Management Spec.

6

Integrated Graphics Subsystem

6.1 Introduction

This chapter describes graphics subsystem that is integrated into the Q35 GMCH component. This graphics subsystem employs the use of system memory to provide efficient, economical 2D and 3D performance.

The SFF and CMT systems may be upgraded/modified by:

- Installing a PCIe x16 graphics card (disables the integrated graphics controller)
- Installing a DVI ADD2 into the PCIe x16 slot (to supplement the integrated graphics controller)

or

- Installing a graphics card in a PCIe x1 slot (disables the integrated controller.

This chapter covers the following subjects:

- Functional description (6.2)
- Display Modes (6.3)
- Upgrading (6.4)
- Monitor connectors (6.5)

6.2 Functional Description

The Intel Q35 GMCH component includes an Intel Integrated Graphics Media Accelerator 3100 controller (Figure 6-1). This integrated graphics controller (IGC) operates internally of the PCIe x16 bus and can directly drive an external, analog multi-scan monitor at resolutions up to and including 2048 x 1536 pixels. The IGC includes a memory management feature that allocates portions of system memory for use as the frame buffer and for storing textures and 3D effects.

The IGC provides two SDVO channels that are multiplexed through the PCIe graphics interface. These SDVO ports may be used by an Advanced Digital Display (ADD2) card installed in the PCI-E x16 graphics slot in driving two digital displays with a 200-megapixel clock.

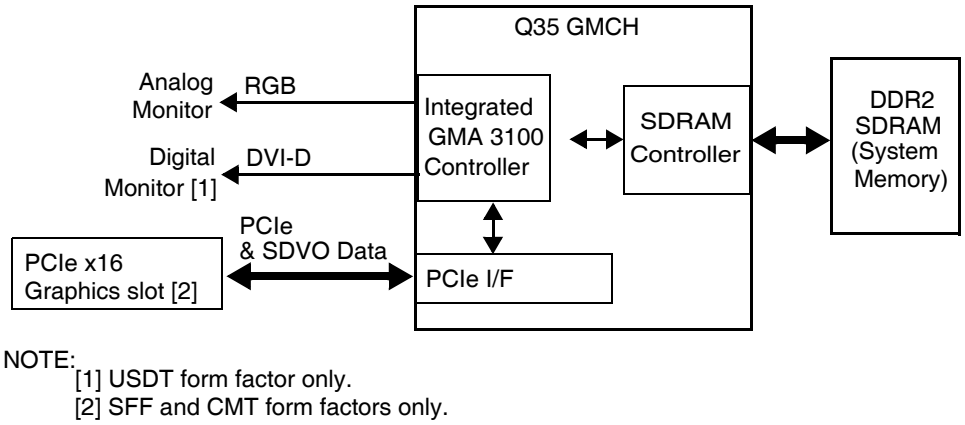


Figure 6-1. Q35 IGC, Block diagram

The IGC provides the following features:

- Rapid pixel and texel rendering using four pipelines that allow 2D and 3D operations to overlap, speeding up visual effects, reducing the amount of memory for texture storage
- Zone rendering for optimizing 3D drawing, eliminating the need for local graphics memory by reducing the bandwidth
- Dynamic video memory allocation, where the amount of memory required by the application is acquired (or released) by the controller
- Intelligent memory management allowing tiled memory addressing, deep display buffering, and dynamic data management
- Provides two serial digital video out (SDVO) channels for use by an appropriate ADD2 accessory card (SFF and CMT form factors only)
- Drives a DVI monitor directly (USDT form factor only)

The IGC includes 2D and 3D accelerator engines working with a deeply-pipelined pre-processor. Hardware cursor and overlay generators are also included as well as a legacy VGA processor core. The controller supports three display devices:

- One progressive-scan analog monitor
- Up to two additional video displays with the installation of an optional Advanced Digital Display (ADD2) card in the PCI Express x16 graphics slot.

The controller can support LVDS, TMDS, or TV output with the proper encoder option.

Special features of the integrated graphics controller include:

- 400-MHz core engine
- 350-MHz 24-bit RAMDAC
- 2D engine supporting GDI+ and alpha stretch blithering up to 2048 x 1536 w/32-bit color @ 75 Hz refresh (QVGA)
- 3D engine supporting Z-bias and up to 1600 x 1200 w/32-bit color @ 85 hz refresh

The IGC uses a portion of system memory for instructions, textures, and frame (display) buffering. Using a process called Dynamic Video Memory Technology (DVMT), the controller dynamically allocates display and texture memory amounts according to the needs of the application running on the system.

The total memory allocation is determined by the amount of system memory installed in a system. The video BIOS pre-allocates 8 megabytes of memory during POST. System memory that is pre-allocated is not seen by the operating system, which will report the total amount of memory installed **less** the amount of pre-allocated memory.

The IGC will use, in standard VGA/SVGA modes, pre-allocated memory as a true dedicated frame buffer. If the system boots with the OS loading the IGC Extreme Graphics drivers, the pre-allocated memory will then be re-claimed by the drivers and may or may not be used by the IGC in the “extended” graphic modes. However, it is important to note that pre-allocated memory is available only to the IGC, not to the OS.

The Q35's DVMT function is an enhancement over the Unified Memory Architecture (UMA) of earlier systems. The DVMT of the Q35 selects, during the boot process, the maximum graphics memory allocation possible according on the amount of system memory installed:

Table 6-1.
IGC Standard 2D Display Modes

SDRAM Installed	Maximum Memory Allocation
128 to 256 megabytes	8-32 MB
257 to 511 megabytes	8-64 MB
>512 megabytes	8-128 MB

The actual amount of system memory used by the IGC in the “extended” or “extreme” modes will increase and decrease dynamically according to the needs of the application. The amount of memory used solely for graphics (video) may be reported in a message on the screen, depending on the operating system and/or applications running on the machine.

For viewing the maximum amount of available frame buffer memory MS Windows go to the Control Panel and select the Display icon, then **> Settings > Advanced > Adapter**.

The Microsoft Direct Diagnostic tool included in most versions of Windows may be used to check the amount of video memory being used. The Display tab of the utility the "Approx. Total Memory" label will indicate the amount of video memory. The value will vary according to OS.

Some applications, particularly games that require advanced 3D hardware acceleration, may not install or run correctly on systems using the IGC.

6.3 Display Modes

The IGC supports the following standard display modes for 2D video displays:

Table 6-2.
IGC Standard 2D Display Modes

Resolution	Maximum Refresh Rate	
	Analog Monitor	Digital Monitor
640 x 480	85 Hz	60 Hz
800 x 600	85 Hz	60 Hz
1024 x 768	85 Hz	60 Hz
1280 x 720	85 Hz	60 Hz
1280 x 1024	85 Hz	60 Hz
1440 x 900	85 Hz	60 Hz
1600 x 900	85 Hz	60 Hz
1600 x 1200	85 Hz	60 Hz
1680 x 1050	85 Hz	60 Hz
1920 x 1080	85 Hz	60 Hz
1920 x 1200	85 Hz	60 Hz
1920 x 1440	85 Hz	60 Hz
2048 x 1536	75 Hz	60 Hz

The highest resolution available will be determined by the following factors:

- Memory speed and amount
- Single or dual channel memory
- Number and type of monitors

6.4 Upgrading

The PCIe x16 slot of SFF and CMT systems can accept a normal-layout Advanced Digital Display 2 (ADD2) or a full-size PCIe x16 graphics controller card. The USDT system with a PCIe x16 riser card installed can accept a reverse-layout Advanced Digital Display 2 (ADD2) or a low-profile PCIe x16 graphics card. Depending on accessory, upgrading through the PCI Express x16 slot can provide digital monitor support and/or dual-monitor support allowing display-cloning or extended desktop functionality. Software drivers may need to be downloaded for specific cards.

Two SDVO channels are provided by the IGC for supporting two digital displays. Existing option cards and drivers support one CRT and digital display. Dual digital display support may be possible with future cards and drivers.

The upgrade procedure is as follows:

1. Shut down the system through the operating system.
2. Unplug the power cord from the rear of the system unit.
3. Remove the chassis cover.
4. Install the graphics or ADD2 card into the PCI Express x16 graphics slot.
5. Replace the chassis cover.
6. Reconnect the power cord to the system unit.
7. Power up the system unit and enter the ROM-based Setup utility using the **F10** key.
8. Select whether to enabled or disable the IGC.
9. Reboot the system.

If a PCIe x1 graphics controller card is installed, the IGC cannot be enabled. The BIOS will detect the presence of the PCIe card and disable the IGC of the Q35 GMCH.

Depending on graphics controllers installed, multiple-monitor configurations are possible. For example, two NVIDIA GF 8400GS 256 MB Dual-Head PCIe x1 graphics controller cards can be installed for multiple-monitor support.

6.5 Monitor Connectors

All form factors provide an analog VGA connector. The USDT system also includes a DVI-D connector for attaching a digital monitor.

6.5.1 Analog Monitor Connector

These systems includes a standard VGA connector (Figure 6-2) for attaching an analog video monitor:

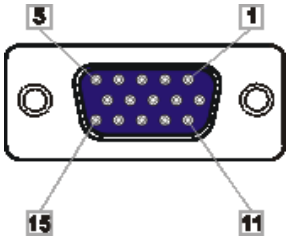


Figure 6-2. DB-15 Analog VGA Monitor Connector, (as viewed from rear of chassis).

Table 6-3.
DB-15 Monitor Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	R	Red Analog	9	PWR	+5 VDC (fused) [1]
2	G	Blue Analog	10	GND	Ground
3	B	Green Analog	11	NC	Not Connected
4	NC	Not Connected	12	SDA	DDC Data
5	GND	Ground	13	HSync	Horizontal Sync
6	R GND	Red Analog Ground	14	VSync	Vertical Sync
7	G GND	Blue Analog Ground	15	SCL	DDC Clock
8	B GND	Green Analog Ground	--	--	--

NOTE:

[1] Fuse automatically resets when excessive load is removed.

6.5.2 Digital Monitor Connector

The USDT system includes a DVI-D connector for attaching a digital video monitor.

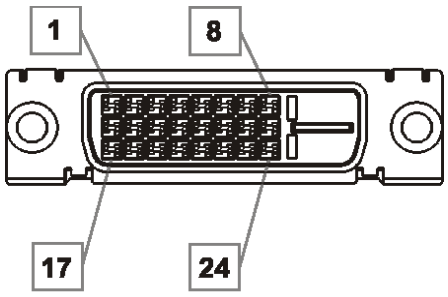


Figure 6-3. DVI-D Digital Monitor Connector, (as viewed from rear of chassis).

Table 6-4.
DB-15 Monitor Connector Pinout

Pin	Signal	Pin	Signal
1	TMDS Data 2-	13	TMDS Data 3+
2	TMDS Data 2+	14	5 VDC
3	TMDS Data 2 & 4 shield	15	Ground
4	TMDS Data 4-	16	Hot plug detect
5	TMDS Data 4+	17	TMDS Data 0-
6	DDC Clock	18	TMDS Data 0+
7	DDC Data	19	TMDS Data 0 & 5 Shield
8	not used	20	TMDS Data 5-
9	TMDS Data 1-	21	TMDS Data 5+
10	TMDS Data 1+	22	TMDS Clock Shield
11	TMDS Data 1 & 3 Shield	23	TMDS Clock +
12	TMDS Data 3-	24	TMDS Clock -

7

Power and Signal Distribution

7.1 Introduction

This chapter describes the power supplies and discusses the methods of general power and signal distribution. Topics covered in this chapter include:

- Power distribution (7.2)
- Power Control (7.3)
- Signal distribution (7.4)

7.2 Power Distribution

Each form factor uses a unique power supply assembly and implements different methods of power generation and distribution. The USDT form factor uses an external ("brick") supply while the SFF and CMT form factors use a power supply unit contained within the system chassis. The subassemblies are not interchangeable between the three form factors.

7.2.1 USDT Power Distribution

The USDT form factor uses an external ("brick") supply that connects to the chassis through a three-conductor cable (Figure 7-1). All voltages required by the processing circuits, peripherals, and storage devices are produced on the system board from the 19.0 VDC produced by the extrernal power supply assembly. The external power supply always produces 19.0 VDC as long as it is connected to an active AC outlet.

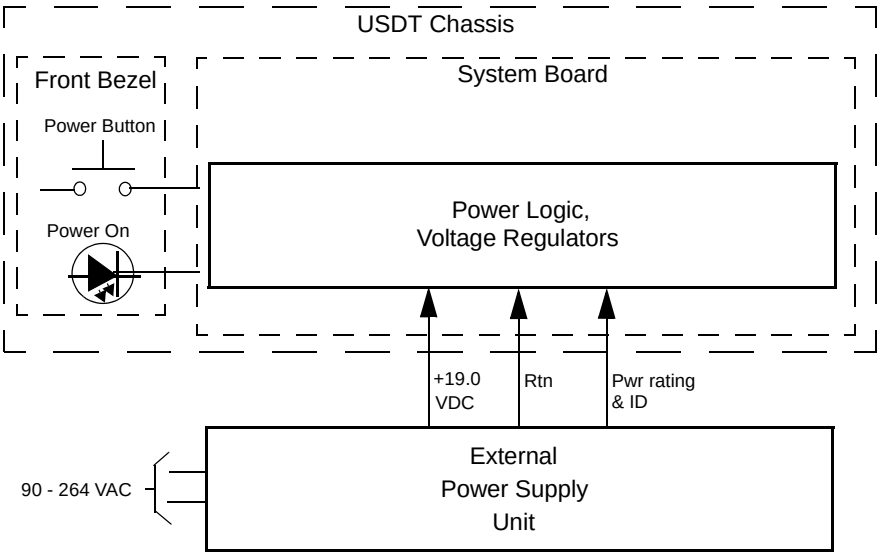


Figure 7-1. USDT Power Generation, Block Diagram

Table 7-1 lists the specifications of the external supply.

Table 7-1.
USDT 135-Watt Power Supply Unit Specifications

Parameter	
Input Line Voltage Range	90–265 VAC
Line Frequency	47–63 Hz
Input Current, Maximum load @ 90 VAC	2.2 A
Output Voltage	19.0 VDC
Output Current, nominal load	3.0 A
Output Current, maximum load	7.1 A
Output Current, peak load (300 ms max) [1]	9.0 A

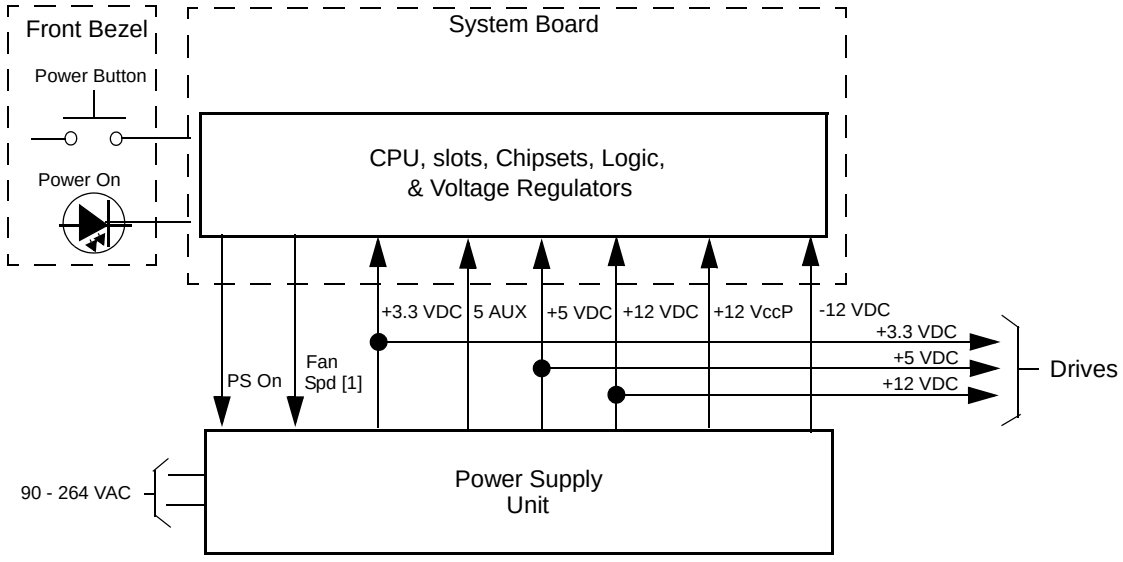
NOTES:

Total continuous power should not exceed 135 watts. Total surge power (<10 seconds w/duty cycle < 5 %) should not exceed 170 watts.

[1] Using 100 VAC input. The output voltage is allowed to drop to a minimum of 15 VDC during the transient period.

7.2.2 SFF Power Distribution

The SFF form factor uses a power supply unit internal to the system chassis. Figure 7-2 shows the block diagram for power generation in the SFF.



NOTE:

[1] Not present on CMT.

Figure 7-2. SFF Power Generation, Block Diagram

Table 7-2 lists the specifications of the SFF power supply unit.

Table 7-2.
SFF 240-Watt Power Supply Unit Specifications

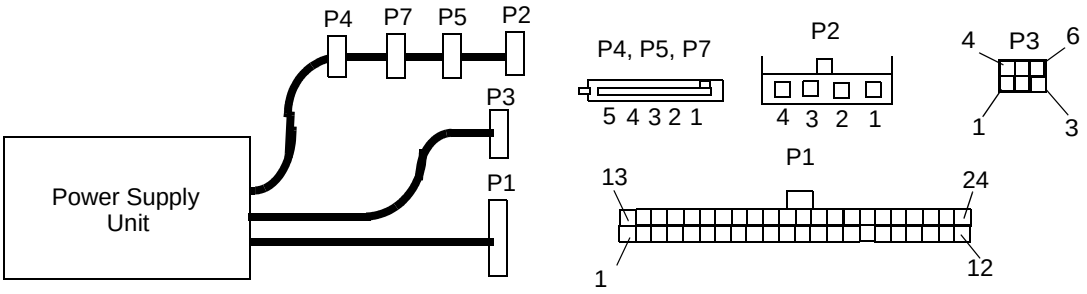
	Range/ Tolerance	Min. Current Loading [1]	Max. Current	Surge Current [2]	Max. Ripple
Input Line Voltage	90–264 VAC	--	--	--	--
Line Frequency	47–63 Hz	--	--	--	--
Input (AC) Current	--	--	5.0 A	--	--
+3.3 VDC Output	± 4%	0.1 A	15.0 A	15.0 A	50 mV
+5.08 VDC Output	± 3.3 %	0.3 A	17.0 A	17.0 A	50 mV
+5.08 AUX Output	± 3.3 %	0.0 A	3.0 A	3.5 A	50 mV
+12 VDC Output	± 5 %	0.1 A	7.5 A	9.0 A	120 mV
+12 VDC Output (Vcpu)	± 5 %	0.1 A	11.0 A	14.5 A	120 mv
-12 VDC Output	± 10 %	0.0 A	0.15 A	0.15 A	200 mV

NOTES:

Total continuous power should not exceed 240 watts. Total surge power (<10 seconds w/duty cycle < 5 %) should not exceed 260 watts.

[1] The minimum current loading figures apply to a PS On start up only.

Figure 7-3 shows the power supply cabling for the SFF system.



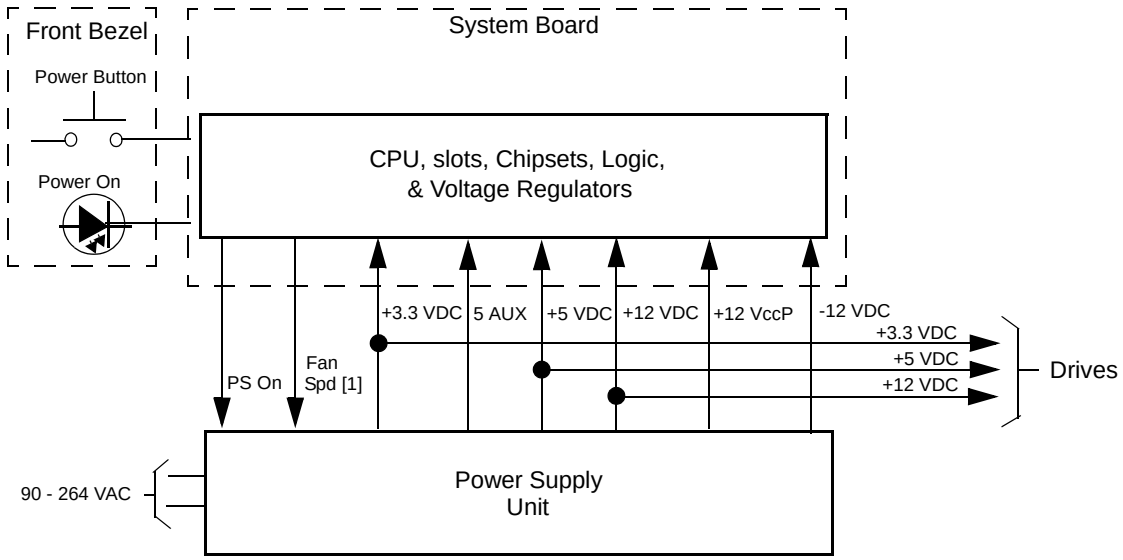
Conn	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 12
P1	+5 aux	RTN	+ 5	+5	PS On	RTN	Pwr Gd	+3.3	+3.3	Tach	RTN	Fan
P1 [1]	+12	+5 sns	RTN	+5	+5	+3.3	RTN	+3.3 sns	+3.3	+3.3	RTN	-12
P2	+5	RTN	RTN	+12								
P3	RTN	RTN	RTN	VccP	VccP	+12						
P4, 5, 7	+3.3	RTN	+5	RTN	+12							

Connectors not shown to scale.
All + and - values are VDC.
RTN = Return (signal ground)
sns = sense
GND = Power ground
RS = Remote sense
FC = Fan command
FO = Fan off
FSpd = Fan speed
FS = Fan Sink
POK = Power OK (power good)
VccP = +12 for CPU
[1] This row represents pins 13–24 of connector P1

Figure 7-3. SFF Power Cable Diagram

7.2.3 CMT Power Distribution

The CMT form factor uses a power supply unit internal to the system chassis. Figure 7-4 shows the block diagram for power generation in the CMT.



NOTE:
[1] Not present on CMT.

Figure 7-4. CMT Power Generation, Block Diagram

Table 7-3 lists the specifications for the 365-watt power supply used in the CMT form factor.

Table 7-3.
CMT 365-Watt Power Supply Unit Specifications

	Range or Tolerance	Min. Current Loading [1]	Max. Current	Surge Current [2]	Max. Ripple
Input Line Voltage:					
115–230 VAC (auto-ranging)	90–264 VAC	--	--	--	--
Line Frequency	47–63 Hz	--	--	--	--
Input (AC) Current	--	--	6.0 A	--	--
+3.3 VDC Output	± 4 %	0.10 A	24.0 A	24.0 A	50 mV
+5.08 VDC Output	± 3.3 %	0.30 A	19.0 A	19.0 A	50 mV
+5.08 AUX Output	± 3.3 %	0.00 A	3.00 A	3.00 A	50 mV
+12 VDC Output	± 5 %	0.20 A	12.0 A	14.5 A	120 mV
+12 VDC Output (Vcpu)	± 5 %	0.00 A	14.5 A	17.5 A	200 mv
-12 VDC Output	± 10 %	0.00 A	0.15 A	0.15 A	200 mV

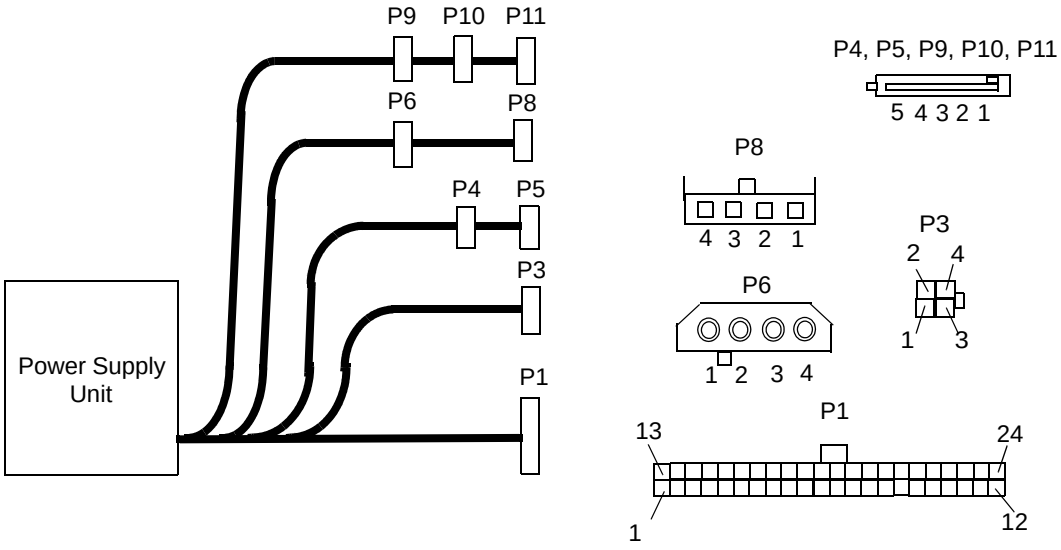
NOTES:

Total continuous output power should not exceed 365 watts. Maximum surge power should not exceed 385 watts.. Maximum combined power of +5 and +3.3 VDC is 160 watts.

[1] Minimum loading requirements must be met at all times to ensure normal operation and specification compliance.

[2] Maximum surge duration for +12Vcpu is 1 second with 12-volt tolerance +/- 10%.

Figure 7-5 shows the power supply cabling for CMT systems.



Conn	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 12
P1	+3.3	+3.3	RTN	+5	RTN	+5	RTN	POK	5 aux	+12	+12	+3.3
P1 [1]	+3.3	-12	RTN	PS On	RTN	RTN	RTN	Open	+5	+5	+5	RTN
P3	RTN	RTN	VccP	VccP								
P4, 5, 9, 10, 11	+3.3	RTN	+5.08	RTN	+12							
P6	+12	RTN	RTN	+5								
P8	+5	RTN	RTN	+12								

NOTES:

Connectors not shown to scale.
All + and - values are VDC.
RTN = Return (signal ground)
GND = Power ground
RS = Remote sense
POK = Power ok (power good)
FC = Fan Command
[1] This row represents pins 13–24 of connector P1.

Figure 7-5. CMT Power Cable Diagram

7.2.4 Energy Star Compliancy

The standard power supply unit for SFF and CMT systems is Energy Star 3.0-compliant. An Energy Star 4.0 (80 Plus-compliant) power supply unit is used for the SFF and CMT form factors in select configurations. The standard USDT power supply unit is compliant with the Energy Star 4.0 specification.

7.3 Power Control

The generation of +3, +5, and ±12 VDC is controlled digitally with the PS On signal. When the PS On signal is asserted, all DC voltages are produced. When PS On is de-asserted, only auxiliary power (+5 AUX) is generated. The +5 AUX voltage is always produced as long as the system is connected to a live AC source.

7.3.1 Power Button

The PS On signal is typically controlled through the Power Button which, when pressed and released, applies a negative (grounding) pulse to the power control logic on the system board. The resultant action of pressing the power button depends on the state and mode of the system at that time and is described as follows:

Table 7-4.
Power Button Actions

System State	Pressed Power Button Results In:
Off	Negative pulse, of which the falling edge results in power control logic asserting PS On signal to Power Supply Assembly, which then initializes. ACPI four-second counter is not active.
On, ACPI Disabled	Negative pulse, of which the falling edge causes power control logic to de-assert the PS On signal. ACPI four-second counter is not active.
On, ACPI Enabled	Pressed and Released Under Four Seconds: Negative pulse, of which the falling edge causes power control logic to generate SMI-, set a bit in the SMI source register, set a bit for button status, and start four-second counter. Software should clear the button status bit within four seconds and the Suspend state is entered. If the status bit is not cleared by software in four seconds PS On is de-asserted and the power supply assembly shuts down (this operation is meant as a guard if the OS is hung). Pressed and Held At least Four Seconds Before Release: If the button is held in for at least four seconds and then released, PS On is negated, de-activating the power supply.

A dual-color LED located on the front panel (bezel) is used to indicate system power status. The front panel (bezel) power LED provides a visual indication of key system conditions listed as follows:

Table 7-5.
Power Button Actions

Power LED	Condition
Steady green	Normal full-on operation
Blinks green @ 0.5 Hz	Suspend state (S1) or suspend to RAM (S3)
Blinks red 2 times @ 1 Hz [1]	Processor thermal shut down. Check air flow, fan operation, and CPU heat sink.
Blinks red 3 times @ 1 Hz [1]	Processor not installed. Install or reseat CPU.
Blinks red 4 times @ 1 Hz [1]	Power failure (power supply is overloaded). Check storage devices, expansion cards and/or system board (CPU power connector P3).
Blinks red 5 times @ 1 Hz [1]	Pre-video memory error. Incompatible or incorrectly seated DIMM.
Blinks red 6 times @ 1 Hz [1]	Pre-video graphics error. On system with integrated graphics, check/replace system board. On system with graphics card, check/replace graphics card.
Blinks red 7 times @ 1 Hz [1]	PCA failure. Check/replace system board.
Blinks red 8 times @ 1 Hz [1]	Invalid ROM (checksum error). Reflash ROM using CD or replace system board.
Blinks red 9 times @ 1 Hz [1]	System powers on but fails to boot. Check power supply, CPU, system board.
Blinks red 10 times @ 1 Hz [1]	Bad option card.
No light	System dead. Press and hold power button for **less** than 4 seconds. If HD LED turns green then check voltage select switch setting or expansion cards. If no LED light then check power button/power supply cables to system board or system board.

NOTE:

[1] Will be accompanied by the same number of beeps, with 2-second pause between cycles. Beeps stop after 5 cycles.

7.3.2 Wake Up Events

The PS On signal can be activated with a power "wake-up" of the system due to the occurrence of a magic packet, serial port ring, or PCI power management event (PME). These events can be individually enabled through the Setup utility to wake up the system from a sleep (low power) state.

Wake-up functionality requires that certain circuits receive auxiliary power while the system is turned off. The system unit must be plugged into a live AC outlet for wake up events to function. Using an AC power strip to control system unit power will disable wake-up event functionality.

The wake up sequence for each event occurs as follows:

Wake-On-LAN

The network interface controller (NIC) can be configured for detection of a "Magic Packet" and wake the system up from sleep mode through the assertion of the PME- signal on the PCI bus. Refer to Chapter 5, "Network Support" for more information.

Modem Ring

A ring condition on a serial port can be detected by the power control logic and, if so configured, cause the PS On signal to be asserted.

Power Management Event

A power management event that asserts the PME- signal on the PCI bus can be enabled to cause the power control logic to generate the PS On. Note that the PCI card must be PCI ver. 2.2 (or later) compliant to support this function.

7.3.3 Power Management

These systems include power management functions designed to conserve energy. These functions are provided by a combination of hardware, firmware (BIOS) and software. The system provides the following power management support:

- ACPI v2.0 compliant (ACPI modes C1, S1, and S3-S5,)
- APM 1.2 compliant
- U.S. EPA Energy Star 3.0 and 4.0 compliant

Table 7-6 shows the comparison in power states.

Table 7-6.
System Power States

Power State	System Condition	Power Consumption	Transition To S0 by [2]	OS Restart Required
G0, S0, D0	System fully on. OS and application is running, all components.	Maximum	N/A	No
G1, S1, C1, D1	System on, CPU is executing and data is held in memory. Some peripheral subsystems may be on low power. Monitor is blanked.	Low	< 2 sec after keyboard or pointing device action	No
G1, S2/3, C2, D2 (Standby/or suspend)	System on, CPU not executing, cache data lost. Memory is holding data, display and I/O subsystems on low power.	Low	< 5 sec. after keyboard, pointing device, or power button action	No
G1, S4, D3 (Hibernation)	System off. CPU, memory, and most subsystems shut down. Memory image saved to disk for recall on power up.	Low	<25 sec. after power button action	Yes
G2, S5, $D3_{cold}$	System off. All components either completely shut down or receiving minimum power to perform system wake-up.	Minimum	<35 sec. after power button action	Yes
G3	System off (mechanical). No power to any internal components except RTC circuit. [1]	None	—	—

NOTES:

Gn = Global state.

Sn = Sleep state.

Cn = ACPI state.

Dn = PCI state.

[1] Power cord is disconnected for this condition.

[2] Actual transition time dependent on OS and/or application software.

7.4 Signal Distribution

Table 7-7 lists the reference designators for LEDS, connectors, headers, and switches used on the system boards for systems covered in this guide. Unless otherwise indicated, components are used on all system boards.

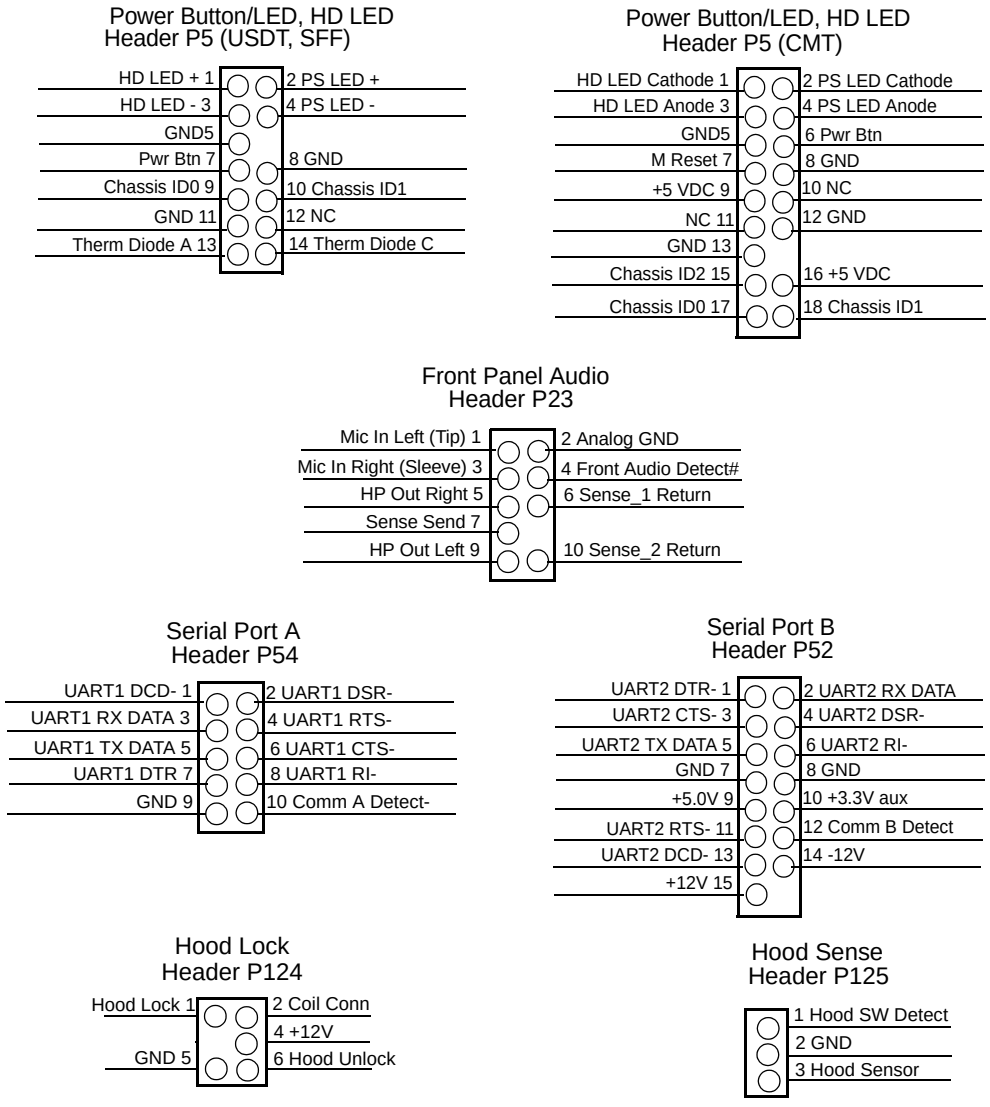
Table 7-7.
System Board Component Designations

Designator	Component function	Notes
CR1	+5 VDC LED	
E1	Descriptor table override header	
E14	SPI ROM boot block header	
E49 / JP49	Password clear header / jumper	
J9	Stacked RJ-45 & dual USB connectors	
J10	Stacked quad USB connectors	
J20	PCI 2.3 connector	SFF & CMT only
J21	PCI 2.3 connector	CMT only
J22	PCI 2.3 connector	CMT only
J31	PCIe x1 connector	SFF & CMT only
J32	PCIe x1 connector	SFF & CMT only
J41	PCIe x16 (graphics) connector	SFF & CMT only
J50	Parallel port, DB-25 connector	SFF & CMT only
J68	Stacked keyboard, mouse PS/2 connectors	
J69	VGA monitor DB-15 connector	
J78	Stacked audio line-in, headphone/line-out 1/8” jacks	
J103	DC input	USDT only
P1	Power supply connector	SFF & CMT only
P3	Vccp (PWRCPU) header	
P5	Control panel (power button, power LED) header	
P6	Internal speaker header	
P8	CPU fan header	
P9	Chassis fan, primary, header	
P10	Diskette drive connector	SFF & CMT only
P20	PATA (IDE), primary, connector	n/a
P21	PATA (IDE), secondary, connector	USDT only
P23	Front panel audio header	
P24	Front panel USB header	
P52	Serial port, secondary, header	SFF & CMT only
P53	Serial port, primary connector	CMT only
P54	Serial port, primary header	SFF only
P60	SATA0 (controller 1, primary) connector (dark blue)	
P61	SATA1 (controller 1, secondary) connector (white)	SFF & CMT only
P62	SATA4 (controller 2, primary) connector (light blue)	SFF & CMT only
P63	SATA5 (controller 2, secondary) connector (orange)	CMT only
P70	CPU fan, primary header	CMT only
P124	Hood lock header	
P125	Hood sense header	
P126	Parallel port header	USDT only
P150	Media reader header	

Table 7-7. *(Continued)*
System Board Component Designations

SW50	Clear CMOS switch	
XMM1	Memory slot (black)	
XMM2	Memory slot (white)	
XMM3	Memory slot (white)	SFF & CMT only
XMM4	Memory slot (white)	SFF & CMT only
XU1	Processor socket	
XB2	Battery socket	

Figure 7-6 shows pinouts of headers used on the sytem boards.



NOTE:

No polarity consideration required for connection to speaker header P6.
NC = Not connected

Figure 7-6. System Board Header Pinouts

8

SYSTEM BIOS

8.1 Introduction

The System Basic Input/Output System (BIOS) of the computer is a collection of machine language programs stored as firmware in read-only memory (ROM). The system BIOS includes such functions as Power-On Self Test (POST), PCI device initialization, Plug 'n Play support, power management activities, and the Setup utility. The firmware contained in the system BIOS ROM supports the following operating systems and specifications:

- DOS 6.2
- Windows 2000, XP, and Vista (Home and Professional versions)
- Windows NT 4.0 (SP6 required for PnP support)
- OS/2 ver 2.1 and OS/2 Warp
- SCO Unix
- DMI 2.1
- Intel Wired for Management (WfM) ver. 2.2
- Alert Standard Format (ASF) 2.0
- ACPI and OnNow
- SMBIOS 2.4
- Intel PXE boot ROM for the integrated LAN controller
- BIOS Boot Specification 1.01
- Enhanced Disk Drive Specification 3.0
- "El Torito" Bootable CD-ROM Format Specification 1.0
- ATAPI Removeable Media Device BIOS Specification 1.0

The BIOS firmware is contained in a 1024 x 8 (8 Mb) flash ROM part. The runtime portion of the BIOS resides in a 128KB block from E0000h to FFFFFh.

This chapter includes the following topics:

- ROM flashing (8.2)
- Boot functions (8.3)
- Client management functions (8.4)
- SMBIOS support (8.5)
- USB legacy support (8.6)
- Management engine functions (8.7)

8.2 ROM Flashing

The system BIOS firmware is contained in a flash ROM device that can be re-written with new BIOS code using a flash utility locally (with F10 setup), with the HPQFlash program in a Windows environment, or with the FLASHBIN.EXE utility in a DOS or DOS-like environment.

8.2.1 Upgrading

Upgrading the BIOS is not normally required but may be necessary if changes are made to the unit's operating system, hard drive, or processor. All System BIOS upgrades are available directly from HP. Flashing is done either locally through F10 setup, the HPQFlash program in a Windows environment, or with the FLASHBIN.EXE utility in a DOS or DOS-like environment. Flashing may also be done by deploying either HPQFlash or FLASHBIN.EXE through the network boot function.

This system includes 64 KB of write-protected boot block ROM that provides a way to recover from a failed flashing of the system BIOS ROM. If the system BIOS ROM fails the flash check, the boot block code provides the minimum amount of support necessary to allow booting the system from the diskette drive and re-flashing the system BIOS ROM with a CD, USB, or diskette.

8.2.2 Changeable Splash Screen

A corrupted splash screen may be restored by reflashing the BIOS image through F10 setup, running HPQFlash, or running FLASHBIN.EXE. Depending on the system, changing (customizing) the splash screen may only be available with asistance from HP.

The splash screen (image displayed during POST) is stored in the system BIOS ROM and may be replaced with another image of choice by using the Image Flash utility (Flashi.exe). The Image Flash utility allows the user to browse directories for image searching and pre-viewing. Background and foreground colors can be chosen from the selected image's palette.

The splash screen image requirements are as follows:

- Format = Windows bitmap with 4-bit RLE encoding
- Size = 424 (width) x 320 (height) pixels
- Colors = 16 (4 bits per pixel)
- File Size = < 64 KB

The Image Flash utility can be invoked at a command line for quickly flashing a known image as follows:

```
>\Flashi.exe [Image_Filename] [Background_Color] [Foreground_Color]
```

The utility checks to insure that the specified image meets the splash screen requirements listed above or it will not be loaded into the ROM.

8.3 Boot Functions

The BIOS supports various functions related to the boot process, including those that occur during the Power On Self-Test (POST) routine.

8.3.1 Boot Device Order

The default boot device order is as follows:

1. CD-ROM drive (EL Torito CD images)
2. Diskette drive (A:)
3. USB device
4. Hard drive (C:)
5. Network interface controller (NIC)

The above order assumes all devices are present in the initial configuration. If, for example, a diskette drive is not initially installed but added later, then drive A would be added to the end of the order (after the NIC)

The order can be changed in the ROM-based Setup utility (accessed by pressing F10 when so prompted during POST). The options are displayed only if the device is attached, except for USB devices. The USB option is displayed even if no USB storage devices are present. The hot IPL option is available through the F9 utility, which allows the user to select a hot IPL boot device.

8.3.2 Network Boot (F12) Support

The BIOS supports booting the system to a network server. The function is accessed by pressing the F12 key when prompted at the lower right hand corner of the display during POST. Booting to a network server allows for such functions as:

- Flashing a ROM on a system without a functional operating system (OS).
- Installing an OS.
- Installing an application.

These systems include, as standard, an integrated Intel 82562-equivalent NIC with Preboot Execution Environment (PXE) ROM and can boot with a NetPC-compliant server.

8.3.3 Memory Detection and Configuration

This system uses the Serial Presence Detect (SPD) method of determining the installed DIMM configuration. The BIOS communicates with an EEPROM on each DIMM through the SMBus to obtain data on the following DIMM parameters:

- Presence
- Size
- Type
- Timing/CAS latency
- PC133 capability

Refer to Chapter 3, "Processor/Memory Subsystem" for the SPD format and DIMM data specific to this system.

The BIOS performs memory detection and configuration with the following steps:

1. Program the buffer strength control registers based on SPD data and the DIMM slots that are populated.
2. Determine the common CAS latency that can be supported by the DIMMs.
3. Determine the memory size for each DIMM and program the GMCH accordingly.
4. Enable refresh.

8.3.4 Boot Error Codes

The BIOS provides visual and audible indications of a failed system boot by using the system's power LED and the system board speaker. The error conditions are listed in the following table.

Table 8-1
Boot Error Codes

Visual (power LED)	Audible (speaker)	Meaning
Blinks red 2 times @ 1 Hz	None	Processor thermal shut down. Check air flow, fan operation, and CPU heat sink.
Blinks red 3 times @ 1 Hz	None	Processor not installed. Install or reseat CPU.
Blinks red 4 times @ 1 Hz	None	Power failure (power supply is overloaded). Check storage devices, expansion cards and/or system board (CPU power connector P3).
Blinks red 5 times @ 1 Hz	5 beeps	Pre-video memory error. Incompatible or incorrectly seated DIMM.
Blinks red 6 times @ 1 Hz	6 beeps	Pre-video graphics error. On system with integrated graphics, check/replace system board. On system with graphics card, check/replace graphics card.
Blinks red 7 times @ 1 Hz	7 beeps	PCA failure. Check/replace system board.
Blinks red 8 times @ 1 Hz	8 beeps	Invalid ROM (checksum error). Reflash ROM using CD or replace system board.
Blinks red 9 times @ 1 Hz	9 beeps	System powers on but fails to boot. Check power supply, CPU, system board.
Blinks red 10 times @ 1 Hz	None	Bad option card.

8.4 Client Management Functions

Table 8-2 provides a partial list of the client management BIOS functions supported by the systems covered in this guide. These functions, designed to support intelligent manageability applications, are HP-specific unless otherwise indicated.

Table 8-2.
Client Management Functions (INT15)

AX	Function	Mode
E800h	Get system ID	Real, 16-, & 32-bit Prot.
E813h	Get monitor data	Real, 16-, & 32-bit Prot.
E814h	Get system revision	Real, 16-, & 32-bit Prot.
E816h	Get temperature status	Real, 16-, & 32-bit Prot.
E817h	Get drive attribute	Real
E818h	Get drive off-line test	Real
E819h	Get chassis serial number	Real, 16-, & 32-bit Prot.
E820h [1]	Get system memory map	Real
E81Ah	Write chassis serial number	Real
E81Bh	Get hard drive threshold	Real
E81Eh	Get hard drive ID	Real
E827h	DIMM EEPROM Access	Real, 16-, & 32-bit Prot.

NOTE:
[1] Industry standard function.

All 32-bit protected-mode functions are accessed by using the industry-standard BIOS32 Service Directory. Using the service directory involves three steps:

1. Locating the service directory.
2. Using the service directory to obtain the entry point for the client management functions.
3. Calling the client management service to perform the desired function.

The BIOS32 Service Directory is a 16-byte block that begins on a 16-byte boundary between the physical address range of 0E0000h-0FFFFFh.

The following subsections provide a brief description of key Client Management functions.

8.4.1 System ID and ROM Type

Diagnostic applications can use the INT 15, AX=E800h BIOS function to identify the type of system. This function will return the system ID in the BX register. Systems have the following IDs and ROM family types:

Table 8-3
System ID Numbers

System (Form Factor)	System ID	Subsystem Device ID
USDT	0AA4h	281Ah
SFF	0AA8h	2818h
CMT:	0AACh	2819h

NOTE: For all systems, BIOS ROM Family = 786F1, PnP ID = CPQ0968, and Subsystem vendor ID = 103Ch.

The ROM family and version numbers can be verified with the Setup utility or the System Insight Manager or Diagnostics applications.

8.4.2 Temperature Status

The BIOS includes a function (INT15, AX=E816h) to retrieve the status of a system's interior temperature. This function allows an application to check whether the temperature situation is at a Normal, Caution, or Critical condition.

8.4.3 Drive Fault Prediction

The BIOS directly supports Drive Fault Prediction for IDE (ATA)-type hard drives. This feature is provided through two Client Management BIOS calls. Function INT 15, AX=E817h is used to retrieve a 512-byte block of drive attribute data while the INT 15, AX=E81Bh is used to retrieve the drive's warranty threshold data. If data is returned indicating possible failure then the following message is displayed:

1720-SMART Hard Drive detects imminent failure

8.5 SMBIOS

In support of the DMI specification, PnP functions 50h and 51h are used to retrieve the SMBIOS data. Function 50h retrieves the number of structures, size of the largest structure, and SMBIOS version. Function 51h retrieves a specific structure. This system supports SMBIOS version 2.4 and the structure types listed in the following table:

Table 8-3
System ID Numbers

Type	Data
0	BIOS Information
1	System Information
2	Base board information
3	System Enclosure or Chassis
4	Processor Information
7	Cache Information
8	Port Connector Information
9	System Slots
13	BIOS Language Information
15	System Event Log Information
16	Physical Memory Array
17	Memory Devices
19	Memory Array Mapped Addresses
20	Memory Device Mapped Addresses
31	Boot Integrity Service Entry Point
32	System Boot Information

System information on these systems is handled exclusively through the SMBIOS.

8.6 USB Legacy Support

The system BIOS ROM checks the USB port, during POST, for the presence of a USB keyboard. This allows a system with only a USB keyboard to be used during ROM-based setup and also on a system with an OS that does not include a USB driver.

On such a system a keystroke will generate an SMI and the SMI handler will retrieve the data from the device and convert it to PS/2 data. The data will be passed to the keyboard controller and processed as in the PS/2 interface. Changing the delay and/or typematic rate of a USB keyboard though BIOS function INT 16 is not supported.

8.7 Management Engine Functions

The management engine function of Intel AMT allows a system unit to be managed remotely over a network, where or not the system is powered up or not[1]. The system BIOS can request the management engine to generate the following alerts:

- Temperature alert
- Fan failure alert
- Chassis intrusion alert
- Watchdog timer alert
- No memory installed alert

1.Assumes the unit is connected to an active AC outlet.

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